Code No: H6809/R13

M. Tech. II Semester Regular/ Supplementary Examinations, July-2016

LOW POWER VLSI DESIGN

(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID, VLSI, VLSID, VLSISD and VLSI & ME)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.	a	Explain about switching power dissipation and short circuit power dissipation.	8
	b	Briefly explain about velocity saturation.	4
2.	a	With a neat sketch, explain a variable threshold CMOS inverter circuit.	6
	b	Compare pipelining and parallel processing approaches.	6
3.	a	Write down the differences between carry select adders and carry save adders.	4
	b	Discuss any two types of low voltage low power logic styles.	8
4.	a	Draw the logic circuit of the conventional CMOS full adder and explain about it.	4
	b	Explain the basic theory, operation and performance evaluation of carry look-ahead adders.	8
5.	a	Draw the basic building blocks of the Baugh-Wooley multiplier architecture and explain its operation.	8
	b	Write down the algorithm of Baugh-Wooley multiplier.	4
6.	a	Discuss the types of multiplier architectures.	4
	b	Explain about Booth multiplier.	8
7.	a	Compare SRAM and DRAM.	4
	b	Give a note on future trend and development of ROM.	4
	c	Write down differences between 6T and 4T static RAM cells.	4
8.	a	With a neat diagram, explain the block diagram of DRAM architecture.	6
	b	Discuss low power SRAM technologies with neat diagrams.	6

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