Code No: I4302/R16

M. Tech. I Semester Supplementary Examinations, February-2020

ANALYSIS OF POWER ELECTRONIC CONVERTERS

(Common to PE, P&ID, PE&ED, PE&D, EM&D PE&S and PE&PS)

Time: 3 hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.		Explain the operation of a three-phase full-wave bidirectional controller connected to a star connected resistive load. Draw necessary voltage and current waveforms with $\alpha = 60^0$.	12
2.	a	Discuss extinction angle control method for power factor improvement of a single-phase full-converter.	6
	b	A single-phase full-wave converter has a source of 120 V rms at 60 Hz, an RL load where R = 10 Ω and L=100 mH. With delay angle $\alpha = 60^0$, (i) verify that the load current is continuous. (ii) determine the dc (average) component of the current. (iii) determine the power absorbed by the load.	6
3.		With the help of a neat schematic and waveforms explain the operation of a three-phase boost power factor corrected rectifier.	12
4.	a	What are the differences between voltage-source and current-source inverters?	6
	b	A single-phase full-bridge inverter has a switching sequence that produces a square wave voltage across a series RL load. The switching frequency is 60 Hz, V_{dc} =100 V, R= 10 Ω and L = 25 mH. Determine the amplitudes of the Fourier series terms for the square wave load voltage, the amplitudes of the Fourier series terms for load current, and the power absorbed by the load.	6
5.	a	What are the advantages of a cascaded multilevel inverter?	4
	b	Explain the working of three-level diode-clamped multilevel inverter with the help of a neat schematic and waveforms.	8
6.		Explain the operation of a 12-pulse converter with the help of a neat schematic and waveforms. Show that the lowest order harmonic present in the input current is 11^{th}.	12
7.	a	What is the purpose of feedback diodes in inverters?	5
	b	Explain the operation of a single-phase AC voltage controller with PWM control. Draw the circuit configuration, gating signals, voltage and current waveforms.	7
8.	a	Draw the schematics of cascaded multilevel inverter and flying-capacitors multilevel inverter. Explain the need for multilevel inverters.	6
	b	What does dc-link capacitor voltage unbalance means?	6

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Code No: I6802/R16

M. Tech. I Semester Supplementary Examinations, February-2020

VLSI TECHNOLOGY AND DESIGN

Common to VLSI&ES (68), ES&VLSI (48), VLSID &ES (77), ES &VLSID (81), VLSI (57), VLSID (72), VLSI System Design (61), VLSI & Micro Electronics (76), DECS (38), Digital Systems & Computer Electronics (06), ECE (70), DECE (37) and I&CS (27)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.	a	Explain the following terms in IC fabrication process (i) Lithography (ii) Diffusion	6M
	b	Explain the concept of ASIC Design flow along with flow diagram	6M
2.	a	Draw the fabrication process of PMOS transistor and explain each step in detail	6M
	b	Explain the following terms in detail (i)Package selection (ii) Power calculation	6M
3.	a	With neat sketch explain fabrication process of P-well CMOS Processes in detail	6M
	b	Explain the concept of mixed signal interfaces along with one example	6M
4.	a	Derive the different Basic Electrical Properties of MOS and Bi-CMOS circuits in detail	6M
	b	Define Scaling and explain the importance of Scaling in MOS transistor in detail	6M
5.	a	Explain the following terms in detail (i) Switch Logic (ii) Gate Logic	6M
	b	Explain the concept of subsystem design in VLSI design along with one example	6M
6.		List out different Floor planning methods used in VLSI Design and explain each one in detail	12M
7.		Explain the following terms in detail (i)Register transfer design (ii) High level synthesis	12M
8.	a	Explain the procedure How Architecture of chip can be tested? Give some example	6M
	b	What is routing? Explain with some suitable example. How it is optimized?	6M

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