Code No: RT31041 **R13** **SET - 1**

III B. Tech I Semester Supplementary Examinations, February-2022

PULSE AND DIGITAL CIRCUITS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A (22 Marks)

1.	a)	Write short notes on Ringing Circuit.	[3M]
	b)	Write the differences between clipping and clamping.	[4M]
	c)	Sketch the piece-wise linear diode characteristics.	[4M]
	d)	What is meant by triggering? Why it is needed?	[4M]
	e)	Write the differences between voltage time base generator and current time base generator.	[4M]
	f)	Write the disadvantages of two diode sampling gate.	[3M]

PART –B (48 Marks)

2.	a)	Discuss about RL Low pass circuit and RL High pass circuit.	[8M]
	b)	An ideal 2 μs pulse is fed to an amplifier. Calculate and plot the output waveform when the upper 3-dB frequency is i) 5 MHz and ii) 0.05 MHz.	[8M]
3.	a)	State and prove clamping circuit theorem.	[8M]
	b)	Design a diode clamper to restore the negative peaks of the input signal to zero level. Use a silicon diode with R_f = 50 Ω and R_r = 400 kΩ. The frequency of the input signal is 5 kHz.	[8M]
4.	a)	Explain about transistor switching times.	[8M]
	b)	Draw the circuit diagram of two input TTL NAND gate and explain its operation.	[8M]
5.	a)	Explain about direct connected binary. Write the advantages and disadvantages of it.	[8M]
	b)	Design a collector coupled one-shot with a gate width of 3 ms using n-p-n transistors. Assume necessary data.	[8M]
6.	a)	With a neat sketch, explain about transistor miller time base generator.	[8M]
	b)	Discuss about Transistor Current Time Base Generator.	[8M]
7.	a)	What is meant by synchronization? Why it is needed? Explain.	[8M]
	b)	Explain how pedestal can be reduced in gate circuit?	[8M]

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