Code No: RT31041 **R13** SET - 1

III B. Tech I Semester Regular/Supplementary Examinations, October/November - 2016
PULSE AND DIGITAL CIRCUITS
(Comm. to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What is meant by linear wave shaping?	[3M]
	b)	Draw a circuit to transmit that part of a sine wave, which is below + 6 V.	[4M]
	c)	How the junctions of transistor are biased for closed switch and open switch.	[3M]
	d)	Write the applications of Schmitt trigger?	[4M]
	e)	Define the Transmission error and explain its significance.	[4M]
	f)	What is meant by sampling gate and give its applications?	[4M]

PART -B

2	a)	Discuss about response of high pass circuit for exponential input.	[8M]
	b)	A square wave whose peak to peak amplitude is 4 V extends ±2 V with respect to ground. The duration of the positive section is 0.3 s and that of the negative section is 0.1 s. If this waveform is impressed upon an RC differentiating network whose time constant is 0.3 s, what are the steady state maximum and minimum values of the output waveform?	[8M]
3	a)	Explain the working of transistor clipper.	[8M]
	b)	A symmetrical 50 Hz square wave whose peak to peak excursions are ± 100 V with respect to ground is to be negatively clamped at 25 V. Draw the necessary circuit diagram and output waveform for this purpose.	[8M]
4	a)	Compare different logic families	[6M]
	b)	Design and Explain CMOS NAND gate.	[10M]
5	a)	Derive the expression for frequency of oscillation of an a stable multi vibrator.	[8M]
	b)	Design a Schmitt trigger circuit for the following specification: UTP = 8 V, LTP = 5 V, V_{CC} = 15V, I_C (sat) = 2 mA, h_{FE}(min) = 25.	[8M]
6	a)	Explain about Exponential sweep circuit and derive the expression for Slope error.	[8M]
	b)	Find the component values of a bootstrap sweep generator, Given V_{CC} = 18 V, I_C(sat) = 2 mA and h_{FE}(min) = 30.	[8M]
7	a)	Explain how mono stable multi vibrator is used as frequency divider?	[8M]
	b)	Explain about unidirectional diode sampling gate. Write its advantages and disadvantages.	[8M]

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Code No: RT31041 **R13** SET - 2

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2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What is the condition for low pass circuit to act as integrator?	[3M]
	b)	What are the applications of voltage comparators?	[4M]
	c)	Explain the dependence of V_{CE} (sat) on temperature.	[4M]
	d)	What is the purpose of commutating capacitors?	[3M]
	e)	Draw the circuit diagram of a sweep circuit using a transistor switch. Also sketch its output waveform.	[4M]
	f)	Write the applications of sampling gates.	[4M]

PART -B

2	a)	Explain the response of high pass circuit for square wave input.	[8M]
	b)	A square wave whose peak to peak amplitude is 4 V extends ±2 V with respect to ground. The duration of the positive section is 0.1 s and that of the negative section is 0.3 s. If this waveform is impressed upon an RC integrating network whose time constant is 0.3 s, what are the steady state maximum and minimum values of the output waveform?	[8M]
3	a)	With neat circuit diagram, explain the working of an emitter coupled clipper.	[8M]
	b)	Explain the clamping circuit considering the source resistance and the diode forward resistance.	[8M]
4	a)	Explain about Diode forward recovery time and Diode reverse recovery time.	[8M]
	b)	Compare the various logic families.	[8M]
5	a)	With neat circuit diagram, Explain the working of fixed bias bistable multi vibrator.	[8M]
	b)	Calculate the component values of a mono stable multi vibrator developing an output pulse of 500 μs duration. Assume h_{FE}(min) = 25, I_{CE}(sat) = 5 mA, V_{CC} = 10 V and V_{BB} = -4V.	[8M]
6	a)	List out the various methods to generate a time base waveform.	[8M]
	b)	The specifications of UJT are given as η =0.6, Vv = 2 V, R_{BB} = 5 kΩ, Iv = 1.5 mA, I_P = 8 μA and V_{BB} = 18 V. Calculate the component values of the UJT sweep circuit to generate an output sweep frequency of 10 kHz with sweep amplitude of 12 V.	[8M]
7	a)	Explain the synchronization of a sweep circuit with symmetrical signals.	[8M]
	b)	With neat circuit diagram, Explain bidirectional sampling gate using transistors.	[8M]

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Code No: RT31041 **R13** SET - 3

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Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What is the condition for High pass circuit to act as differentiator?	[3M]
	b)	Write the difference between clipping and clamping.	[4M]
	c)	Define rise time and storage time.	[4M]
	d)	What is meant by triggering? Why it is needed?	[4M]
	e)	Write the relationship between Transmission error and displacement error.	[4M]
	f)	What is pedestal?	[3M]

PART -B

2	a)	Sketch the response of low pass RC circuit for step input and derive the expression for rise time.	[8M]
	b)	An ideal 2μs pulse is fed to an amplifier. Calculate and plot the output waveform when the upper 3-dB frequency is (**a**) 5 MHz and (**b**) 0.05 MHz	[8M]
3	a)	State and prove clamping circuit theorem.	[8M]
	b)	A symmetrical 50 Hz square wave whose peak to peak excursions are ± 100 V with respect to ground is to be positively clamped at 25 V. Draw the necessary circuit diagram and output waveform for this purpose.	[8M]
4	a)	Explain the design of transistor switch.	[8M]
	b)	Draw the circuit diagram of Two in put TTL NAND gate and explain its operation.	[8M]
5	a)	Explain about direct connected binary. Write the advantages and disadvantages of it.	[8M]
	b)	Design a stable multi vibrator to generate a square wave of 1 kHz frequency with a duty cycle of 25% using silicon n-p-n transistors with h_{FE}(min) = 40.	[8M]
6	a)	Explain the basic principles of Miller and Bootstrap time base generators.	[8M]
	b)	Discuss about Transistor Current Time Base Generator.	[8M]
7	a)	What is meant by synchronization? Why it is needed? Explain.	[8M]
	b)	Explain about four diode sampling gate.	[8M]

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Code No: RT31041 **R13** SET - 4

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2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Write short notes on Ringing Circuit.	[3M]
	b)	What is the difference between linear wave shaping and non linear wave shaping?	[4M]
	c)	Sketch the piece-wise linear diode characteristics.	[3M]
	d)	What is clamping theorem?	[4M]
	e)	Write the difference between voltage time base generator and current time base generator.	[4M]
	f)	Write the disadvantages of two diode sampling gate.	[4M]

PART -B

2	a)	Discuss about RL Low pass circuit and RL High pass circuit.	[8M]
	b)	A 1 KHz square wave output from an amplifier has rise time t_r = 350 ns and tilt = 5 %. Determine the upper and lower 3- dB frequencies.	[8M]
3	a)	Explain the working of negative clamping circuit.	[8M]
	b)	Design a diode clamper to restore the negative peaks of the input signal to zero level. Use a silicon diode with R_f = 50 Ω and R_r = 400 kΩ. The frequency of the input signal is 5 kHz.	[8M]
4	a)	Explain about transistor switching times.	[8M]
	b)	Draw the circuit diagram of Inverter Using CMOS logic and explain its operation.	[8M]
5	a)	With neat circuit diagram, Explain the working of the emitter – coupled binary.	[8M]
	b)	Design a collector coupled one-shot with a gate width of 3 ms using n-p-n transistors. Assume necessary data.	[8M]
6	a)	With neat sketch, explain about transistor miller time base generator.	[8M]
	b)	Derive the expression for sweep time of sweep circuit using UJT.	[8M]
7	a)	Explain about phase delay and phase jitters.	[8M]
	b)	Explain how pedestal can be reduced in gate circuit.	[8M]

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