Code No: RT31042 **R13** SET - 1

III B. Tech I Semester Supplementary Examinations, May - 2019

LINEAR IC APPLICATIONS

(Common to Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) List the basic processes used in the silicon planer technology. [3M]
   b) Draw the equivalent circuit of an ideal OP-AMP. [4M]
   c) List the important features of an instrumentation amplifier. [4M]
   d) The resonant frequency f_o of a band pass filter is 1khz and its bandwidth is 3 kHz. Find the value of Q. [3M]
   e) Discuss the operation of a FSK generator using 555 timers. [4M]
   f) Explain about basic DAC technologies with schematic diagram. [4M]

PART -B

2. What is an integrator circuit? Discuss the relative advantages and disadvantages if IC'S over discrete assembly. How will you make a monolithic IC explain in detail? [16M]

3. a) Explain about input offset voltage with a neat diagram. [8M]
   b) Define Slew rate. How it effect the op-amp performance? Explain. [8M]

4. a) With a neat diagram explain about the voltage to current converter in details. [8M]
   b) Describe the working of practical differentiator circuit. Derive the expression for output voltage. [8M]

5. a) With a neat diagram explain the band reject filter. Derive the expression for output voltage. [8M]
   b) Design a first order low pass filter for a high cut-off frequency of 2 kHz and pass band gain of 2. [8M]

6. The free running frequency of a 565 PLL is 100 kHz, the filter capacitor is 2μF and supply voltage is ± 6V. Compute the lock in range, capture range frequency and value of external components R_T and C_T. [16M]

7. a) With a neat diagram explain about the counter type A/D converter in detail. [8M]
   b) Determine the output voltages caused by each bit in a 6-bit ladder if the input levels are 0=0v and 1=+16v. Determine the resolution and full-scale output of this circuit. Find out the voltage from the above ladder for a digital input of 101011. [8M]

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