**R13**

**SET - 1**

### III B. Tech I Semester Supplementary Examinations, May - 2018
## LINEAR IC APPLICATIONS
(Common to Electronics and Communication Engineering, Electronics and Instrumentation Engineering and Electronics and Computer Engineering)

Time: 3 hours                                                                                               Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**
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#### PART –A

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|---|---|---|---|
| 1 | a) | What are the properties of dual input unbalanced output differential amplifier? | [3M] |
| | b) | Define CMRR of op-amp. | [3M] |
| | c) | Derive the gain of non inverting amplifier. | [4M] |
| | d) | Draw the schematic of a second order High-pass filter and sketch the frequency response. | [4M] |
| | e) | Mention the applications of 555 timer used as Monostable and Astable operations. | [4M] |
| | f) | What are the specifications of AD 574 (12 bit ADC) | [4M] |

#### PART -B

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|---|---|---|---|
| 2 | a) | Analyze the dual input balanced output configuration of differential amplifier using DC. | [8M] |
| | b) | Write and Explain about DC coupling and cascaded differential amplifier stages. | [8M] |
| | | | |
| 3 | a) | Briefly explain the various types of IC packages. Mention the criteria for selecting an IC package. | [8M] |
| | b) | With a neat sketch explain the frequency compensation using pole – zero method. | [8M] |
| | | | |
| 4 | a) | Explain, how to obtain triangular wave using a square wave generator. | [8M] |
| | b) | Draw the circuit of Log and Anti log Amplifiers explain its operation. | [8M] |
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| 5 | a) | Compare Active filters with passive filters. | [6M] |
| | b) | Discuss in detail about band pass and band reject filters. | [10M] |
| | | | |
| 6 | a) | Explain the operation of astable multivibrator using 555 IC Timer. | [8M] |
| | b) | Design a Mono stable multivibrator for 3ms pulse width. | [8M] |
| | | | |
| 7 | a) | Draw the circuit of weighted resistor DAC and derive expression for output analog voltage Vo. | [10M] |
| | b) | Find out step size and analog output for 4 -bit R-2R ladder DAC, when input is 0 1 1 1 and 1 1 1 1, assume Vref=+5V. | [6M] |

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