R13

SET - 1

III B. Tech I Semester Regular/Supplementary Examinations, October/November - 2016
LINEAR IC APPLICATIONS
(Comm to ECE, EIE and E.Comp.E)

Time: 3 hours   Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**
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PART –A

1	a)	What is the main advantage of constant current bias over emitter bias in differential amplifiers?	[4M]
	b)	What are the temperature grades of integrated circuits?	[3M]
	c)	What are the effects of voltage series feedback in Op-amp?	[4M]
	d)	Draw a sample and hold circuit.	[3M]
	e)	What is the purpose of low pass filter in a phase locked loop?	[4M]
	f)	Define settling time and stability of data converters.	[4M]

PART -B

2	a)	Draw the ac equivalent circuit of dual input balanced output differential amplifier and derive the expressions for small signal voltage gain, input resistance and output resistance.	[10M]
	b)	Compare the above results with a dual input unbalanced differential amplifier.	[6M]
3	a)	List out the ideal characteristics of an operational amplifier.	[3M]
	b)	Define slew rate of an Op-amp and explain its significance in the dynamic characteristicsof an Op-amp.	[8M]
	c)	An op-amp has a slew rate of 2V/µs. What is the maximum frequency of an output sinusoid of peak value 5V at which the distortion sets in due to the slew rate limitation	[5M]
4	a)	Design a practical op-amp differentiator circuit for the frequency of 1KHz and explain its frequency response.	[8M]
	b)	Design a Schmitt trigger circuit for UTP and LTP of +3V and -3V respectively. Explain its hysteresis curve.	[8M]
5	a)	Design a first order band pass filter with lower cutoff frequency of 100Hz and a higher cutoff frequency of 1KHz. The pass band gain should be 4. Calculate the 'Q' of the filter.	[12M]
	b)	Compare butterworth and chebyshev filter responses.	[4M]
6	a)	Explain the operation of Monostable multivibrator using 555 timer. Derive the expression for quasi stable state time period of a Monostable multivibrator using 555 timer.	[10M]
	b)	Draw the block diagram of PLL and explain importance of each block	[6M]
7	a)	Describe the operation of successive approximation type analog to digitalconverter.	[8M]
	b)	Draw the circuit of weighted resistor DAC and derive expression for output-analog voltage.	[8M]

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PART –A

1 a) What is the importance of DC coupling in Op-amp internal structure?   [4M]
   b) Define slew rate? Give typical value for 741C Op-amp.   [3M]
   c) Draw and explain voltage transfer characteristics of an ideal Op-amp.   [4M]
   d) Explain relationship between Q and bandwidth of a bandpass active filter.   [4M]
   e) What is the purpose of reset pin in a 555 timer IC?   [4M]
   f) Explain monotonicity of a D/A converter   [3M]

PART -B

2 a) Draw the ac equivalent circuit of dual input unbalanced output differential   [10M]
      amplifier and derive the expressions for small signal voltage gain, input resistance
      and output resistance.
   b) Compare the above results with a dual input balanced differential amplifier.   [6M]

3 a) Explain the basic internal block diagram of a typical operational amplifier.   [8M]
   b) Explain the measurement procedure for input and output offset voltages of a   [8M]
      practical Op-amp.

4 a) Explain the operation of a grounded load V to I converter using op-amp.   [8M]
   b) Design any stable multi vibrator circuit using 741 op-amp for the frequency of   [8M]
      10KHz square wave. Assume necessary data.

5 a) Classify the filters based on range of frequencies, frequency response, type of   [8M]
      components used and type of input signal.
   b) Design a first order low pass filter with cutoff frequency of 1KHz and pass band [8M]
      gain of 11. Also draw its frequency response.

6 a) Define lock-in range and capture range of a PLL   [6M]
   b) Draw the internal diagram of a 555 timer IC and explain significance of each pin. [10M]

7 a) With a clear block diagram explain the data conversion procedure for dual slope   [8M]
      ADC.
   b) List the advantages of dual slope ADC compared to other ADC models.   [8M]

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SET - 3

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Time: 3 hours   Max. Marks: 70

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2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What is the use of level translator in the Op-amp internal structure?	[3M]
	b)	What is CMRR? Give an ideal value for an Op-amp.	[4M]
	c)	Explain why an open-loop Op-amp is unsuitable for linear applications?	[4M]
	d)	Classify band pass active filters according to their Q values.	[4M]
	e)	Draw the dc output voltage of VCO versus frequency characteristic of a PLL indicating the capture and lock range clearly.	[4M]
	f)	Explain linearity with respect to data converters	[3M]

PART -B

2	a)	What is an op-amp? Draw the equivalent circuit of a typical op-amp and explain.	[6M]
	b)	Draw the ac equivalent circuit of single input balanced output differential amplifier and derive the expressions for small signal voltage gain.	[10M]
3	a)	With suitable sketches, explain the measurement procedure for the slew rate and CMRR.	[8M]
	b)	What is input bias current and explain the bias current compensation in an inverting and non-inverting amplifier circuits?	[8M]
4	a)	Design an Opamp based circuit to produce an output $-(V_1+2V_2-5V_3)$, where V_1, V_2 and V_3 are the input voltages.	[8M]
	b)	What is the difference between conventional rectifier and precision rectifier?	[8M]
5	a)	Design a first order high pass filter with a cutoff frequency of 1KHz and pass band gain of 11. Also draw its frequency response.	[10M]
	b)	List the differences between the frequency responses of first order filters and second order filters.	[6M]
6	a)	Design a symmetrical square wave generator with 1KHz frequency and 5V peak value using 555 timer IC. Assume necessary data.	[8M]
	b)	Explain the application of PLL as a FSK demodulator.	[8M]
7	a)	Explain in detail with a neat circuit diagram the operation of 3-bit parallel ADC.	[8M]
	b)	List the advantages and disadvantages of flash type ADC.	[8M]

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PART –A

1	a)	Draw the configuration of single input unbalance out put differential amplifier.	[3M]
	b)	What is the importance of Gain-Bandwidth product of an Op-amp?	[4M]
	c)	What are the effects of voltage shunt feedback in Op-amp?	[4M]
	d)	What are the advantages of active filter over a passive filter?	[4M]
	e)	Illustrate the pin configuration of 555 timer IC mentioning the name of eachpin.	[4M]
	f)	Define resolution of a D/A converter.	[3M]

PART -B

2	a)	Explain the operation of Level translator with relevant diagrams and expressions.	[6M]
	b)	Draw the small signal equivalent circuit of differential amplifier circuit and obtain the expressions for common mode gain and differential mode gain.	[10M]
3	a)	An OP-AMP has a differential gain equal to 90 dB and CMRR is 100 dB. If the two input voltages are 3µV, and 2 µV respectively, calculate the differential mode output and common mode output voltages.	[8M]
	b)	What is thermal drift and mention the techniques to minimize the effect of thermal drift?	[8M]
4	a)	Design a Schmitt trigger circuit to convert 5V, 1 KHz sinusoidal signal to square wave using 741C. Draw its transfer characteristics, Input and output waveforms.	[8M]
	b)	Draw the circuit diagram of a practical log amplifier and obtain an expression for its output voltage.	[8M]
5	a)	Explain the term frequency scaling with a suitable example.	[6M]
	b)	Design a wide band-pass filter with f_H=200Hz ,f_L=1KHz and a pass-band gain=4. Draw the frequency response and calculate Q factor for the filter.	[10M]
6	a)	Explain the operation of an astable multivibrator using 555 timer. Derive the expression for on and off state time periods.	[8M]
	b)	With a clear block diagram explain frequency multiplier using PLL.	[8M]
7	a)	Explain in detail with a neat circuit diagram the operation of anR-2R ladder, DAC digital to analog converter.	[8M]
	b)	List the advantages of R-2R ladder DAC compared to weighted resistor DAC	[8M]

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