

III B. Tech I Semester Supplementary Examinations, October/November - 2018
LINEAR IC APPLICATIONS

(Common to Electronics and Communication Engineering, Electronics and Instrumentation
 Engineering and Electronics and Computer Engineering)

Time: 3 hours

Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
 2. Answering the question in **Part-A** is compulsory
 3. Answer any **THREE** Questions from **Part-B**

PART -A

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|---|----|---|------|
| 1 | a) | What is a Level translator? | [3M] |
| | b) | Define slew rate and PSRR | [4M] |
| | c) | Draw the circuit of (i) voltage to current (V to I) converter with grounded load
(ii) current to voltage (I to V) converter with grounded load | [4M] |
| | d) | Mention the applications of Analog switches. | [4M] |
| | e) | Define lock range, capture range and pull-in-time. | [4M] |
| | f) | Draw the circuit of R-2R ladder DAC. | [3M] |

PART -B

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|---|----|---|-------|
| 2 | a) | What is an Op-amp. Briefly explain the necessity and function of different stages of an Op-amp with respect to its block schematic. | [8M] |
| | b) | Explain the DC analysis of single input unbalanced output amplifier. | [8M] |
| 3 | a) | Define and explain the significance of following terms :
i) CMRR ii) Drift | [8M] |
| | b) | List out electrical characteristics of an op-amp. | [8M] |
| 4 | a) | Draw the circuit diagram of instrumentation amplifier using 741 op - amp and explain its operation. | [8M] |
| | b) | With a neat sketch explain the op-amp differentiator circuit. | [8M] |
| 5 | a) | Explain the operation of a sample and hold amplifier. | [10M] |
| | b) | Explain IC1496 balanced modulator with a neat sketch. | [6M] |
| 6 | a) | Explain the operation of Schmitt trigger circuit with input and output waveforms. | [8M] |
| | b) | Describe PLL with block diagram. Also discuss applications of PLL in phase detector and voltage controlled oscillator. | [8M] |
| 7 | a) | Explain the working of a dual slope A/D converter. | [8M] |
| | b) | Enlist the advantages and disadvantages of dual slope ADC. | [8M] |
