Code No: RT31042 **R13** SET - 1

III B. Tech I Semester Supplementary Examinations, October/November - 2020

LINEAR IC APPLICATIONS

(Common to Electronics and Communication Engineering, Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A (22 Marks)

1. a) List the advantages of integrated circuits. [3M]
   b) A differential dc amplifier has a differential mode gain of 100 and a common mode gain 0.01. What is its CMRR in dB? [4M]
   c) Draw the circuit of a summing operational amplifier using inverting amplifier configuration. [4M]
   d) Determine the order of a low pass Butterworth filter that is to provide 40 dB attenuation at $W/W_h=2$. [4M]
   e) What is a VCO? Give two applications of VCO. [3M]
   f) Which is the fastest ADC and why it is so? [4M]

PART –B (48 Marks)

2. a) Differentiate between SSI, MSI, LSI and VLSI. [8M]
   b) Explain planar technology for device fabrication. [8M]

3. a) Draw the block schematic of an op-amp and explain the functions of each block. [8M]
   b) The two input terminals of an op-amp are connected to voltage signals of strength 745µV and 740 µV respectively. The gain of the OP-AMP in differential mode is $5x10^5$ and its CMRR is 80dB. Calculate the output voltage and percentage error due to common mode. [8M]

4. a) Explain how an op-amp can be used as integrator? Also derive expression for the output. [8M]
   b) Design an instrumentation amplifier to have a variable differential gain in the range 5-200. Use a 50 kilo-ohm potentiometer. [8M]

5. a) Design a first order low pass filter for a high cut-off frequency of 2 kHz and Pass band gain of 2. [8M]
   b) Draw the circuit diagram of first order high pass filter and its frequency response. Derive the expression for output voltage. [8M]

6. a) Compute the free running frequency f_o, lock in range and capture range of PLL565. Assume R_T=20 k-ohm, C_T=0.01µF, C=1µF and supply voltage is ± 6v. [8M]
   b) Draw and explain the circuit of astable multivibrator using 555 timer. [8M]

7. a) With a neat diagram explain the successive approximation converter in detail. [8M]
   b) Consider a 10 bit D/A converter having a reference voltage of 10 V. What is the Binary digital input needed to get 4.5 V output? What outputs are obtained from the converter for the inputs of (i) binary 0010110101 (ii) decimal 520? [8M]

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