Code No: RT31044 **R13** SET - 1

III B. Tech I Semester Supplementary Examinations, May - 2019

DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS

(Common to Electronics and Communication Engineering,
Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Give the syntax and structure of a package in VHDL.	[4M]
	b)	Define logic synthesis.	[3M]
	c)	What are the commercial ROM types?	[3M]
	d)	Explain the terms i) Noise margin ii) Transition time with respect to CMOS logic	[4M]
	e)	Write a VHDL program for 2x4 Decoder.	[4M]
	f)	Write VHDL code for D Flip Flop with asynchronous reset using behavioral modeling.	[4M]

PART -B

2	a)	What is binding? Discuss binding between entity and Architecture.	[8M]
	b)	Explain about dataflow design elements of VHDL.	[8M]
3		Write short notes on (i) technology libraries. (ii)Place and route (iii) Netlist formats.	[16M]
4	a)	With the help of logic diagram explain the function of PAL with one example.	[8M]
	b)	With the help of timing waveforms, explain the read and write operations of static RAM.	[8M]
5	a)	Explain about CMOS/TTL interfacing.	[8M]
	b)	Discuss about the fastest logic family and mention the typical values of its various Parameters.	[8M]
6	a)	Write a data-flow style VHDL program for 4:1 MUX.	[8M]
	b)	Explain about the Dual Priority Encoder with neat diagram.	[8M]
7	a)	Write a VHDL code for Ring counter.	[8M]
	b)	Explain the different Modes of Operation of Shift Registers.	[8M]

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