Code No: **RT31044** **R13** SET - 1

III B.Tech I Semester Supplementary Examinations, August - 2021

DIGITAL SYSTEM DESIGN AND DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A **(22 Marks)**

1. a) Define Verilog HDL. [3M]
   b) What is functional Gate level verification? [4M]
   c) What are the differences between SRAM and DRAM? [3M]
   d) Draw the circuit of basic ECL inverter. [4M]
   e) Explain about Barrel Shifter. [4M]
   f) Distinguish between the synchronous and asynchronous counters. [4M]

PART –B **(48 Marks)**

2. a) Discuss about the Libraries and Bindings. [4M]
   b) Using examples, explain about Concurrent and Sequential Statements with syntaxes. [8M]
   c) Explain difference between signal and variable in VHDL. [4M]

3. a) Explain Post Layout Timing Simulation. [8M]
   b) Explain synthesis procedure in Verilog HDL. [8M]

4. a) Explain about PLA design aspects in detail. [8M]
   b) Implement the logic function 'F' using ROM. [8M]
   F = A'BC'+A'BC+AB'C+ABC.

5. a) Explain the differences between DTL, TTL and ECL. [8M]
   b) Explain steady state and dynamic electrical behavior of CMOS. [8M]

6. a) Design a 4×4 combinational multiplier and write the VHDL program in data flow model. [8M]
   b) Explain about simple floating point encoder with an example. [8M]

7. a) Distinguish between latch and flip-flop. Show the logic diagram for both. Explain the operation with the help of function table. [8M]
   b) Draw the logic diagram of 74×163 binary counter and explain its operation. [8M]

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