Code No: RT31044 **R13** SET - 1

III B. Tech I Semester Regular/Supplementary Examinations, October/November - 2016
DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS
(Comm to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Write short note VHDL requirements.	[3M]
	b)	Explain about pull gates VHDL modeling.	[4M]
	c)	How a 2-to-4 decoder can be realized using ROM?	[3M]
	d)	Draw the schematic diagram of a tri-state buffer and explain its operation.	[4M]
	e)	Write a VHDL code for a 4 bit up counter	[4M]
	f)	Compare latches and flip flops.	[4M]

PART -B

2	a)	What are the different data objects supported by VHDL? Explain scalar types with suitable examples.	[8M]
	b)	Write a VHDL Entity and Architecture for the following function. F = a (XOR) b (XOR)c, Also draw the relevant logic diagram.	[8M]
3	a)	When is a label required for a block?	[3M]
	b)	Explain the Functional Gate-Level verification with example.	[8M]
	c)	How does the case statement duffer from the case statement?	[5M]
4	a)	What is the minimum size of a Read Only Memory to realize a binary multiplier of two 4-bit unsigned numbers?	[8M]
	b)	Compare and contrast commercially available Read only memories, PROM, EPROM and EEPROM.	[8M]
5	a)	Discuss about dynamic electrical behavior.	[8M]
	b)	Mention about the merits and demerits of ECL gate	[8M]
6	a)	Discuss about the implementation of comparator using digital IC.	[8M]
	b)	Explain about the Dual Priority Encoder with neat diagram.	[8M]
7	a)	Discuss about the working of Johnson Counter using 74 LS194.	[8M]
	b)	Write a VHDL program to simulate the behavior of a positive edge triggered 'D' flip – flop.	[8M]

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Code No: RT31044 **R13** SET - 2

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PART –A

1	a)	Explain about the Objects and Classes.	[3M]
	b)	Write shot note on Functional Gate-Level verification.	[4M]
	c)	Explain briefly Static RAM Internal structure.	[3M]
	d)	Draw the circuit for CMOS OR-AND-Invert logic gates.	[4M]
	e)	Design a full adder using two half adders. Write its structural code.	[4M]
	f)	Discuss the steps involved in the analysis of sequential circuits.	[4M]

PART -B

2	a)	What statement is primarily used to describe a design in dataflow style?	[4M]
	b)	What is the purpose of the ‘timescale’ compiler derivative? Give an example.	[8M]
	c)	What is wrong with the following continuous assignment? **assign**reset = #2 ^ hwrite_bus;	[4M]
3	a)	Explain the difference between function and procedure supported by VHDL. Give the necessary examples.	[9M]
	b)	Explain data-low design elements of VHDL.	[7M]
4	a)	Explain the operation of Synchronous SRAM with the help of its internal architecture.	[8M]
	b)	Explain the design procedure of 4x4 binary multiplexer using 256x8 ROM	[8M]
5	a)	Write about the totem pole arrangement in case of TTL family.	[8M]
	b)	Differentiate between the TTL and DTL logic families.	[8M]
6		Design 8 bit ALU using digital ICs.	[16]
7		Design a 4 bit synchronous binary even counter and write its behavioural model.	[16]

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Code No: RT31044 **R13** SET - 3

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2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Write short note on package declaration.	[3M]
	b)	Comparison of VHDL and Verilog HDL.	[4M]
	c)	What are the different register types in VHDL?	[3M]
	d)	Explain about CMOS steady state electrical behavior.	[4M]
	e)	Draw the truth table and circuit diagram of a 2-to-4 decoder.	[4M]
	f)	Write a short note on Programmable Array Logic Devices.	[4M]

PART -B

2	a)	Write a short note on Elements of VHDL.	[4M]
	b)	What is the use of packages and libraries in VHDL? Explain with examples.	[12M]
3	a)	Draw the logic diagram of simple8x4 diode ROM and explain its function.	[8M]
	b)	Explain the DRAM read and write cycle timings with help of waveforms.	[8M]
4	a)	With the block diagram of output buffer control portion of an SRAM to describe bi-directional data transfer operations in SRAM.	[8M]
	b)	With the help of timing waveforms, explain read and write operations of DRAM.	[8M]
5	a)	Design 2-input LS-TTL NAND gate and explain its operation. Give the function table, truth table.	[8M]
	b)	Compare CMOS, TTL and ECL with reference to logic levels, DC noise margin, propagation delay and fan-out.	[8M]
6	a)	Design the logic circuit and write a data-flow style VHDL program for the following functions? $F(X) = \sum A,B,C,D(0,1,3,5,14) + d(8,15)$	[8M]
	b)	Write a data-flow style VHDL program for 4:1 MUX.	[8M]
7	a)	Design a self-correcting 4-bit, 4-state ring counter with a single circulating 0 using IC 74LS194.	[8M]
	b)	Explain the different Modes of Operation of Shift Registers.	[8M]

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Code No: RT31044 **R13** SET - 4

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3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Write a syntax of VHDL array declaration.	[3M]
	b)	Write note onConcurrent and Sequential Statements.	[4M]
	c)	Explain different Commercial ROM types.	[3M]
	d)	What are the salient features of TTL logic family?	[4M]
	e)	Write a VHDL code to simulate a full adder circuit.	[4M]
	f)	Write Modes of Operation of Shift Registers.	[4M]

PART –B

2	a)	Explain the terms entity, is, port, in, out and end pertaining to VHDL complier.	[8M]
	b)	Write a VHDL program using all the above terms and explain the same.	[8M]
3	a)	Explain the difference between VHDL program structure and other procedural language program structure.	[8M]
	b)	Write a VHDL program to detect prime number of a 8-bit input.	[8M]
4	a)	List out various types of Read-Only-Memories that are commercially available. Describe the functionality and limitations of each type.	[8M]
	b)	Draw the timing diagram to specify typical timing parameters of an SRAM to perform write operation.	[8M]
5	a)	Write about the TTL to CMOS interfacing.	[8M]
	b)	Discuss about the fastest logic family and mention the typical values of its various parameters.	[8M]
6	a)	Write the disadvantages in implementation of N-bit binary adder using full adders.	[5M]
	b)	Explain the working of carry look ahead adder and its advantages.	[11M]
7	a)	Write a VHDL program to design a modulo-6 counter	[12M]
	b)	Write the differences between flip-flop and latch.	[4M]

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