Code No: RT31044 **R13** SET - 1

III B. Tech I Semester Supplementary Examinations, October/November- 2020

DIGITAL SYSTEM DESIGN AND DIGITAL IC APPLICATIONS

(Common to Electronics and Communication Engineering, Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A (22 Marks)

1. a) Write down the syntax of a VHDL entity declaration. [3M]
   b) What is timing simulation? [4M]
   c) Give the classification of PLDs. [4M]
   d) State the logic levels for typical CMOS logic circuits. [4M]
   e) List out the differences between multiplexer and de-multiplexer. [4M]
   f) Distinguish between a latch and a flip-flop. [3M]

PART –B (48 Marks)

2. a) With suitable example explain PROCESS statement in VHDL. [8M]
   b) What are the various types of objects in VHDL? Explain. [8M]

3. a) With a suitable block diagram explain the logic synthesis process. [8M]
   b) Explain briefly about gate level simulation with a suitable diagram. [8M]

4. a) Design, draw and explain 128x8 ROM using 32x8 ROMs. [8M]
   b) With suitable timing diagrams explain Read and Write operations in DRAM. [8M]

5. a) Explain what is meant by logic family? Construct an Ex-NOR circuit using CMOS transistors and explain its operation. [8M]
   b) Explain the difference between current sinking and current sourcing logic circuits. How they are estimated for CMOS families? [8M]

6. a) Write a VHDL program for 16-bit barrel shifter for left circular shift only. [8M]
   b) Write a VHDL code for four bit parallel adder/subtractor. [8M]

7. a) Explain the operation of a 4 bit synchronous binary counter with the required diagram and waveforms. [8M]
   b) Write a VHDL code for 4-bit Serial-in Parallel-out register. [8M]

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