Code No: RT31044 **R13** SET - 1

III B. Tech I Semester Regular Examinations, November – 2015
DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What are the data types available in VHDL?	[4M]
	b)	What is logic synthesis?	[3M]
	c)	What are the differences between PROM,PLA and PAL	[3M]
	d)	Explain the terms i) Noise margin ii) Transition time with respect to CMOS logic.	[4M]
	e)	Write a VHDL code for 1× 4 demultiplexer?	[4M]
	f)	Convert a D Flip-flop into T flip-flop	[4M]

PART –B

2	a)	Explain about data objects in VHDL.	[4M]
	b)	Explain the structure of various LOOP statements in VHDL with examples.	[8M]
	c)	Give the syntax and structure of a package in VHDL.	[4M]
3	a)	Define simulation? Explain about Gate-level simulation, Behavioral simulation and Functional simulation.	[8M]
	b)	Explain about inertial delay and Transport delay models in VHDL with examples.	[8M]
4	a)	Describe DRAM with an appropriate diagram and explain about its timings.	[8M]
	b)	Compare PROM, PAL and PLA.	[8M]
5	a)	Explain the CMOS circuit behavior with resistive load.	[8M]
	b)	Design a 2-input XOR and XNOR logic gates using CMOS logic.	[8M]
6	a)	Implement the 32 input to 5 output priority encoder using four 74LS148 & gates.	[8M]
	b)	Draw the logic diagram of IC 74180 parity generator checker and explain its operation with the help of a truth table.	[8M]
7	a)	Explain how a JK- flip-flop can be constructed using a T- flip-flop.	[8M]
	b)	Discuss the logic circuit of 74×377 register. Write a VHDL program for the same in structural style.	[8M]

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Code No: RT31044 **R13** SET - 2

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2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What is HDL? Why do you need it?	[3M]
	b)	What is binding?Discuss the binding between library and components.	[4M]
	c)	Distinguish between SRAM and ROM.	[4M]
	d)	What are the advantages and disadvantages of CMOS technology?	[3M]
	e)	Write a VHDL program for 2x4 Decoder	[4M]
	f)	Convert a T flip-flop into a JK Flip-flop	[4M]

PART –B

2	a)	Write a VHDL program for n-bit ripple carry adder	[8M]
	b)	What are different data types available in VHDL? Explain.	[8M]
3	a)	What are the goals and objectives of Global routing and detailed routing?	[8M]
	b)	Explain the following: i) Timing constraints ii) Performance-driven synthesis iii) Circuit – level simulation.	[8M]
4	a)	With the help of timing waveforms, explain the read and write operations of static RAM.	[8M]
	b)	Design a BCD to Gray-code converter using PLA.	[8M]
5	a)	Design a 4 input CMOS OR-AND INVERT gate. Explain the circuit with the help of logic diagram and function table.	[8M]
	b)	Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation.	[8M]
6	a)	Write a VHDL code for 4-bit Look ahead carry generator.	[8M]
	b)	Design a 4×4 combinational multiplier and write the VHDL program in data flow model.	[8M]
7	a)	Design an Excess-3 decimal counter using 74 X 163 and explain the operation with the help of timing waveforms	[8M]
	b)	Give a VHDL code for a 4-bit upcounter with enable and clear inputs.	[8M]

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Code No: RT31044 **R13** SET - 3

III B. Tech I Semester Regular Examinations, November - 2015
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Time: 3 hours Max. Marks: 70

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2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What is Enumeration data type in VHDL? Give examples.	[3M]
	b)	Differentiate between Functions and Procedures in VHDL.	[4M]
	c)	List out the applications of ROM.	[3M]
	d)	Give the logic levels and noise margins of CMOS and TTL families.	[4M]
	e)	Write a VHDL program for 4x1 multiplexer	[4M]
	f)	Convert a T flip-flop into a D Flip-flop	[4M]

PART –B

2	a)	Discuss the binding? Discuss the binding between entity and components.	[8M]
	b)	Explain about signal assignment statements and Variable assignment statements with example.	[8M]
3	a)	What is the importance of time dimension in VHDL and explain its function.	[8M]
	b)	Discuss some of the important factors related to Synthesis.	[8M]
4	a)	Draw the block diagram of Synchronous RAM and explain its operation.	[8M]
	b)	Design an excess-3 to BCD code converter using PLA.	[8M]
5	a)	Design a 4 input CMOS AND-OR-INVERT gate. Explain the circuit with the help of logic diagram and function table.	[8M]
	b)	Explain about the steady state electrical CMOS behaviors for i) Resistive loads ii) Non ideal inputs	[8M]
6	a)	Design a priority encoder for 16 inputs using two 74×148 encoders.	[8M]
	b)	Write the VHDL program for fixed point to floating point conversion.	[8M]
7	a)	Design a 3 bit LFSR counter using 74×194.List out the sequence assuming that the initial state is 111.	[8M]
	b)	Draw the logic diagram of universal shift register and explain its operation.	[8M]

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Code No: RT31044 **R13** SET - 4

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Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**
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PART –A

1	a)	Differentiate between VHDL and Verilog HDL.	[3M]
	b)	Write a test bench for two input XOR gate using VHDL.	[4M]
	c)	What are advantages of Programmable logic devices?	[3M]
	d)	List out the characteristics of ECL.	[4M]
	e)	Write a VHDL program for 4x2 encoder.	[4M]
	f)	Convert a JK Flip-flop into D Flip-flop.	[4M]

PART –B

2	a)	Explain about dataflow design elements of VHDL.	[8M]
	b)	What is binding? Discuss binding between entity and Architecture.	[8M]
3	a)	Write a VHDL program for comparing 8 bit unsigned integers.	[8M]
	b)	Discuss synthesis information from entity with examples.	[8M]
4	a)	Implement the following Boolean functions using a PLA F1(A,B,C)= Σ m(0,1,3,5); F2=(A,B,C)= Σ m(3,5,7).	[8M]
	b)	Determine the ROM size needed to realize the logic function performed by 74×153 and 74×139.	[8M]
5	a)	What is interfacing? Explain interfacing between low voltage TTL and low voltage CMOS logic.	[8M]
	b)	Design a transistor circuit of 2 input ECL NOR gate. Explain the operation with the help of function table.	[8M]
6	a)	Design a full adder using two half adders. Write VHDL program for the above implementation.	[8M]
	b)	Design a 16-bit comparator using 74×85IC's.	[8M]
7	a)	Design a 8 bit parallel-in and serial-out shift register. Explain the operation of the above shift register with the help of timing waveforms.	[8M]
	b)	Design a modulo – 100 counter using two 74 x 163 binary counters.	[8M]

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