III B. Tech I Semester Supplementary Examinations, October/November - 2018 DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS

(Common to Electronics Computer Engineering and Electronics Instrumentation Engineering)

,	Time:	3 hours Max. I	Marks: 70
_		Note: 1. Question Paper consists of two parts (Part-A and Part-B) 2. Answering the question in Part-A is compulsory 3. Answer any THREE Questions from Part-B	
		<u>PART -A</u>	
1	a)	Explain about data objects in VHDL.	[3M]
	b)	Discuss about Technology Libraries.	[4M]
	c)	Explain briefly Static RAM Internal structure.	[4M]
	d)	Explain about CMOS steady state electrical behavior.	[4M]
	e)	Explain the significance of Dual Priority encoder.	[4M]
	f)	Compare latches and flip flops.	[3M]
	,	PART -B	[-]
2	a)	Explain the Packages and Libraries of VHDL?	[8M]
_	b)	Compare and contrast between VHDL and Verilog HDL.	[8M]
3	a)	Explain why place and route tools are used in VHDL with the help of data flow diagram.	v [8M]
	b)	Explain in detail about Post Layout Timing Simulation.	[8M]
1	۵)	Explain the internal structure of DDOM and list its advantages	[OM]
4	a) b)	Explain the internal structure of PROM and list its advantages. Describe DRAM with an appropriate diagram and explain about its timings.	[8M] [8M]
	U)	Describe DRAW with an appropriate diagram and explain about its immigs.	[OIVI]
5	a)	Explain dynamic electrical behavior of a CMOS.	[8M]
	b)	What are the salient features of ECL? and explain its internal structure	[8M]
6	a)	Write the VHDL code for 16 bit barrel shifter.	[8M]
	b)	Design a 4 bit carry look ahead adder using gates and write the VHDL code for it	. [8M]
7	a)	Write a VHDL program to design a modulo-8 counter.	[8M]
,	a) b)	Explain in detail about the working of Johnson Counter using 74 LS194.	[8M]
	0)	Express in detail about the working of volumen daining / Letty i.	[01,1]
