Code No: RT31044 **R13** SET - 1

III B. Tech I Semester Supplementary Examinations, October/November- 2019

DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS

(Common to Electronics and Communication Engineering, Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A (22 Marks)

1.	a)	What do you mean by concurrent statement?	[4M]
	b)	What is net list?	[3M]
	c)	Explain the 2D decoding technique.	[4M]
	d)	State the noise margin for CMOS family.	[3M]
	e)	Briefly discuss about priority encoder.	[4M]
	f)	List out the differences between asynchronous and synchronous counter.	[4M]

PART –B (48 Marks)

2.	a)	With the help of block diagram, explain the program structure of VHDL.	[8M]
	b)	List out the differences between various VHDL functions and procedures with example.	[8M]
3.	a)	Explain the synthesis process with suitable a block diagram.	[8M]
	b)	Explain how a logic level simulation can verify complex circuits compared to other simulations?	[8M]
4.	a)	Explain the internal structure of 64Kx1 DRAM with the help of timing waveforms.	[8M]
	b)	Discuss how PROM, EPROM and EEPROM technologies different from each other?	[8M]
5.	a)	Draw the circuit diagram and functional table of ECL 10K 2-input OR/NOR gate and explain its operation.	[8M]
	b)	Which bipolar family is best suited for LSI? Draw the circuit of a 4-input NAND gate using CMOS transistors.	[8M]
6.	a)	Using a process statement write a VHDL source code for 4 to 1 multiplexer.	[8M]
	b)	Design a function F = ABC+ $(A+B+C)'$ by using IC 74X138.	[8M]
7.	a)	Discuss the logic circuit of IC 74x377 register. Write a VHDL program for the same in structural style.	[8M]
	b)	Draw the logic diagram of 74x74 IC and explain the operation. Develop the VHDL model for this IC.	[8M]

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