Code: 13A05401 **R13**

B.Tech III Year I Semester (R13) Supplementary Examinations June 2017

COMPUTER ORGANIZATION & ARCHITECTURE

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) List out components of a CPU.
(b) Why do you need interfacing in CO?
(c) Write about decimal arithmetic unit.
(d) State various algorithms available for multiplication and division operations.
(e) Explain how shift micro operations.
(f) What are the uses of register transfer language?
(g) Discuss about possible modes of data transfer.
(h) Mention the functions of associative memory.
(i) What is parallel processing?
(j) Describe the need for Inter Processor Communication.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 What is an instruction set? Explain how an instruction set architecture design works.

OR

3 (a) Describe about memory subsystem organization.
(b) Write the differences between RISC and CISC.

UNIT – II

4 (a) Discuss about steps involved in instruction cycle with interrupt enabled.
(b) State any two Floating point Arithmetic operations.

OR

5 (a) Explain the steps needed for storing a single word in memory.
(b) Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation.

UNIT – III

6 (a) Write the procedure to mitigate number of bits in micro instructions.
(b) Explain how control memory functions.

OR

7 What is a micro-operation of list and explain the four categories of the most common micro-operations?

UNIT – IV

8 Construct an associative memory page table with number of words equal to the number of blocks in the main memory.

OR

9 Explain the Strobe Control method of Asynchronous data transfer. What are the disadvantages of this method?

UNIT – V

10 What is pipelining? Name the two pipeline organizations. Explain about the arithmetic pipeline with the help of an example.

OR

11 Describe the need for Inter processor communication. Elaborate the synchronization concept used in Inter processor communication.

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