Code: 13A05401 **R13**

B.Tech III Year I Semester (R13) Regular & Supplementary Examinations November/December 2016

COMPUTER ORGANIZATION & ARCHITECTURE

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) How data is fetched from memory?

(b) What is little endian in multibyte organization?

(c) Consider an instruction **ADD 20(R_1), R_2** and assume that R_1 and R_2 contain 1000 and 1003 respectively. Calculate effective address of operands.

(d) For what reason devices generate interrupts?

(e) Assume that register R_3 contain a binary number 0010 0000 0000. Write single assembly language instruction to make it binary number that is equivalent to decimal 1024.

(f) Draw the basic organization of a micro programmed control unit

(g) In case, if a program does not show locality of reference then, cost of the execution will increase. Why?

(h) What is the problem with the copy-back protocol?

(i) Define data hazard.

(j) Sometimes processors in tightly coupled multiprocessor environment will be idle. Why?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain about levels of programming language.

OR

3 Give a brief note on assemble language instructions.

UNIT – II

4 List and explain the various phases in the instruction execution? Draw and explain how a single-bus data path is organized inside a processor when sequences of instructions are executed.

OR

5 Multiply each of the following pairs of signed 2's compliment numbers using the Booth multiplication and n-bit multipliers. In each case assume that A is multiplicand and B is multiplier.

(i) A=010111 and B=110110. (ii) A=110011 and B=101100.

UNIT – III

6 Present a simple digital computer and show how it is micro programmed.

OR

7 (a) Show the block diagram of hardware that implements the following register transfer statements:

T2=R2 ← R1 , R1 ← R2

(b) Design a 4-bit combinational circuit decremented using four full-adder circuits.

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UNIT – IV

8 Write in detail about modes of I/O transfer.

OR

9 (a) A block-set-associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words.
(i) How many bits are there in a main memory address?
(ii) How many bits are there in each of the TAG, SET, and WORD fields?

(b) A disk unit has 24 recording surfaces. It has a total of 14,000 cylinders. There is an average of 400 sectors per track. Each sector contains 512 bytes of data.
(i) What is the data transfer rate in bytes per second at a rotational speed of 7200 rpm?
(ii) Using a 32-bit word, suggest a suitable scheme for specifying the disk address, assuming that there are 512 bytes per sector.

UNIT – V

10 (a) A program loop ends with a conditional branch to the beginning of the loop. How would you implement this loop on a pipelined computer that uses delayed branching with one delay slot? Under what conditions would you be able to put a useful instruction in the delay slot?

(b) A computer has one delay slot. The instruction in this slot is always executed, but only on a speculative basis. If a branch does not take place, the results of that instruction are discarded. Suggest a way to implement program loops efficiently on this computer.

OR

11 (a) Construct a diagram for a 4 x 4 omega switching network. Show the switch setting required to connect input 3 to output 1.

(b) Define the following terms associated with the multiprocessor:
(i) Mutual exclusion.
(ii) Critical section.
(iii) Hardware lock.
(iv) Semaphore.
(v) Test and set instruction.

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