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C14–EC–**305**

4241

BOARD DIPLOMA EXAMINATION, (C–14)

MARCH/APRIL—2017

DECE—THIRD SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. Subtract the following binary numbers :

(a) 1001_2 from 1011_2

(b) 101_2 from 1001

(c) 11_2 from 10111_2

2. State De Morgan's theorems and give the expressions.

3. Draw the symbol and truth table of exclusive OR gate.

4. List any three logic families.

5. Draw the full-adder circuit by using two half-adders and one OR gate.

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6. State the need of tristate buffer.

7. Explain the need for preset and clear inputs.

8. Draw the logic circuits of NAND and NOR latch.

9. List the types of register.

10. Write any three differences between EEPROM and UVPROM.

PART—B

10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. Convert the following numbers :

(a) $(1011010)_2$ = ( )$_{10}$

(b) $(22\ 4)_8$ = ( )$_{10}$

(c) $(AB3)_{16}$ = ( )$_{10}$

(d) $(47\ 5)_8$ = ( )$_{10}$

(e) $(C3F)_{16}$ = ( )$_{10}$

12. *(a)* Draw the symbols and truth tables of NOT, AND, OR gates.

(b) Simplify the boolean expression

$$Y(A, B, C) \quad m(0, 4, 5, 6, 7)$$

using K-map and draw logic circuit after reduction of Boolean expression.

13. Draw the circuit and explain the working of TTL NAND gate with totem pole output.

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14. *(a)* Draw and explain 2's complement parallel adder/ subtractor circuit. 7

(b) Compare the performance of serial and parallel adder. 3

15. *(a)* Draw and explain decimal to BCD encoder. 7

(b) Mention any three applications of multiplexer circuit. 3

16. Explain the operation of master-slave *J-K* flip flop with neat sketch.

17. Draw and explain the working of universal shift register with circuit and timing diagram.

18. Draw and explain the working of 3-bit up/down asynchronous counter with a circuit.

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