



C14-EC-305

4241

BOARD DIPLOMA EXAMINATION, (C-14)
OCT/NOV—2015
DECE—THIRD SEMESTER EXAMINATION
DIGITAL ELECTRONICS

Time : 3 hours]

[Total Marks : 80

PART—A

3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

1. Convert $(38\ 15)_{10}$ in to binary number.
2. State De Morgan's theorems.
3. Realize the basic gates using NAND gates only.
4. Compare different logic families.
5. State the need for a tri-state buffer.
6. Mention any three applications of multiplexers.
7. Draw T flip-flop using $J-K$ flip flop and write its truth table.
8. Explain briefly the concept of edge triggering in flip-flops.
9. List the four types of shift registers.
10. Compare static RAM and dynamic RAM.

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PART—B

10×5=50

Instructions : (1) Answer *any five* questions.

(2) Each question carries **ten** marks.

11. (a) Simplify the following expression : 6

$$\overline{ABC} \quad \overline{ABC} \quad \overline{ABC} \quad ABC \quad ABC$$

(b) Explain the importance of parity bit. 4

12. (a) Simplify the following Boolean expression : 7

$$Y \quad m(0, 1, 2, 3, 8, 9, 10, 11)$$

(b) What are universal gates and why are they called so? 3

13. Draw Totem pole TTL NAND gate circuit and explain its working.

14. Draw the circuit diagram of 2's complement parallel adder/sub-tractor and explain its working.

15. Draw the circuit diagram of 3 8 decoder and explain its working.

* **16.** Explain the operation of *J-K* master-slave flip-flop with a neat sketch.

17. Explain the working of 4-bit shift right register.

18. (a) Distinguish between EEPROM and UVROM. 5

(b) Draw the circuit diagram of asynchronous decade counter. 5
