



C14-EC-606

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**BOARD DIPLOMA EXAMINATION, (C-14)
MARCH/APRIL—2018
DECE—SIXTH SEMESTER EXAMINATION**

DIGITAL CIRCUIT DESIGN THROUGH VERILOG HDL

Time : 3 hours]

[Total Marks : 80

PART—A

3×10=30

- Instructions :** (1) Answer **all** questions.
(2) Each question carries **three** marks.
(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. What is functional simulation?
2. Write the use of Verilog HDL in VLSI simulation.
3. List layout design rules.
4. What are port connection rules in a module instantiation?
5. Write about the data types, value sets, nets and registers.
6. Write about identifiers and keywords in Verilog.
7. What is User Defined Primitive?

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8. What is hierarchical modeling?
9. Write Verilog code for 3 to 8 decoder using dataflow modeling.
10. Write Verilog code for decade counter using dataflow modeling.

PART—B

10×5=50

Instructions : (1) Answer *any five* questions.
 (2) Each question carries **ten** marks.
 (3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. (a) Explain VLSI design specification and design entry. 5
 (b) Explain stick diagrams. 5
12. Explain all types of operators used in Verilog HDL.
13. (a) Explain the importance of hardware description languages in VLSI design. 5
 (b) Explain defparam and localparam keywords. 5
14. (a) Explain about initial and always statements. 5
 (b) Explain while, for, repeat and forever looping statements. 5
15. Design simple logic circuits for full adder and full subtractor using structural modeling.
16. (a) Design 8 to 3 encoder using behavioural modeling. 5
 (b) Design *J-K* flip-flop with synchronous clock and reset using behavioral modeling. 5

17. Design SISO^{*} shift registers and 4 : 1 multiplexer using dataflow modeling.

18. (a) State and explain finite state machines. 5

(b) Explain the structure of stimulus module. 5

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