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C14-EC-606

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BOARD DIPLOMA EXAMINATION, (C-14)

JUNE—2019

DECE—SIXTH SEMESTER EXAMINATION DIGITAL CIRCUIT DESIGN THROUGH VERILOG HDL

Time : 3 hours] [*Total Marks* : 80

PART—A

3 ×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. What is timing simulation?

2. What are the uses of Verilog HDL in VLSI simulation?

3. Write briefly about stick diagrams

4. LIst the levels of abstraction to represent the internals of a module.

5. Define expressions, operators and operands.

6. List any four data types used in the Verilog HDL.

7. Write briefly about identifying and keywords in verilog

8. What are the advantages of Hierarchical modelling?

9. Write Verilog code for 3 to 8 decoder in behavioral modeling.

10. Write Verilog code for 4 to 1 multiplexer using case statement in behavioral modeling.

PART—B

10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer

11. With a neat diagram, explain different stages in VLSI design flow.

12. *(a)* Explain briefly about below given data types, with two examples for each.

(i) Nets *(ii)* Registers *(iii)* Vectors

(b) Explain differences between modules and module instances in Verilog.

13. Explain the port connection rules in a module instantiation. inverilog with examples.

14. *(a)* Explain blocking and non-blocking procedural allignments.

(b) Give examples for the above.

15. *(a)* Explain sequential and parallel block.

(b) Write any two differences between conditional if statement and case statement.

16. *(a)* Write verilog code for D-Flip flop with synchronous clock and reset. in behavioral modeling.

(b) Write verilog code for Decade counter in behavioral modeling.

17. Explain about RTL and structural level modeling.

18. *(a)* List different state machine.

(b) Explain meelay type of state machine with a block diagram.

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