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C14–EC–606

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## BOARD DIPLOMA EXAMINATION, (C–14)

## OCT/NOV—2018

## DECE—SIXTH SEMESTER EXAMINATION

DIGITAL CIRCUIT DESIGN THROUGH VERILOG HDL

*Time* : 3 hours ] [ *Total Marks* : 80

**PART—A** 3×10=30

***Instructions*** : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

**1.** What is timing simulation?

**2.** What is design entry?

**3.** What is planning placement and routing (PPR)?

**4.** Write the features of Verilog HDL

**5.** Write any three differences between an instantiation and inference of a component.

**6.** Define expressions, operators and operands.

**7.** List the advantages of hierarchical modelling.

**8.** Distinguish between sequential and parallel blocks.

**9.** Write Verilog code for 2-bit comparator using dataflow modelling.

**10.** Write Verilog code for D flip-flop with synchronous clock and reset using dataflow modelling.

## PART—B

10×5=50

***Instructions*** : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

**11.** Explain VLSI design flow.

**12.** Explain four levels of abstraction to represent the internals of a module.

**13.** Explain about system tasks and compiler directives.

**14.** *(a)* Explain conditional statements. 5

*(b)* Explain blocking and non-blocking procedural assignments with examples. 5

**15.** Design logic circuits for half subtractor and full subtractor using structural modelling.

**16.** *(a)* Design RS flip-flip with synchronous clock and reset using behavioural modelling. 5

*(b)* Design 3 to 8 decoder using behavioural modelling. 5

**17.** Design SISO shift registers using behavioural and dataflow modelling.

**18.** *(a)* Write stimulus module for 4 : 1 multiplexer. 5

*(b)* Write stimulus module for JK flip-flop. 5

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