4640

BOARD DIPLOMA EXAMINATION, (C-14) MARCH/APRIL—2021

DEEE - FIFTH SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time: 3 hours [Total Marks: 80

PART—A

 $4 \times 5 = 20$

Instructions:

- (1) Answer any five questions.
- (2) Each question carries **four** marks.
- (3) Answers should be brief and straight to the point and shall not exceed five simple sentences.
- **1.** Draw the logic symbols and truth tables for the AND, OR gates.
- 2. State De-Morgan's theorems.
- 3. Draw the circuit of TTL NAND gate with Totem pole output.
- **4.** List the characteristics of digital ICs.
- **5.** Define the terms power dissipation and propagation delay.
- **6.** Draw the Full Adder using two Half Adders and OR gate.
- 7. List any four applications of Decoders.
- 8. Write the need for CLEAR and PRESET inputs of Flip-Flops.
- **9.** Draw the T-Flip-Flop using JK Flip-Flop.
- 10. Distinguish between RAM and ROM.

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PART—B

Instructions :		(1) Answer any four questions.						
		(2)	Each question	n carries fif t	een mark	S.		
		(3)	Answers sho valuation is t		•			
11.	<i>(i)</i> N	(i) NAND (ii) NOR						6
	• •	•	-Map method, Ising basic gat	. 3	e following	Boolean fu	inction and	Ç
			$Y = \overline{ABC} + \overline{ABC}$	$C + A\overline{B}\overline{C} + A$	BC			
12.	(a) Compare TTL, CMOS and ECL logic families.						5	
	(b) List	any	five IC numbe	rs of 2 inpu	ıt digital IC	C logic gate:	S.	5
	(c) Men	tion	any five chara	acteristics o	f digital IC	S.		5
13.	Draw and explain the working of TTL NAND gate with open colle				n collector.	15		
14.	Draw and explain the operation of 3 × 8 Decoder.							15
15.	Explain the working of serial adder with a block diagram.							15
16.	Draw and explain the level clocked D and T flip-flops with truth tables.						with truth	15
17.	Draw and explain Master-Slave JK flip-flop with its truth tables.						ables.	15
18.	(a) Draw and explain the working of basic dynamic MOS RAM cell.					RAM cell.	Ç	

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(iii) memory capacity.

(b) Briefly explain (i) memory read operation, (ii) access time and

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