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C14–EE–505

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BOARD DIPLOMA EXAMINATION, (C–14)

JUNE—2019

DEEE—FIFTH SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. Draw the logic symbols and truth tables for the following gates.

(a) NAND

(b) NOR

(c) EXOR

2. Subtract 101.11 from 1100.1 by using 2's complement method.

3. Draw the circuit of TTL NAND gate with open collector.

4. List the characteristics of digital ICs.

5. Classify digital logic families.

6. List any three applications of decoders.

7. State the need for a tri-state buffer.

8. Write the need for clear and preset inputs.

9. List any three application of flipflops.

10. List any three common aplications of shift registers.

PART—B

10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer

11. Develop the logic gates AND, OR and NOT by using NAND and FOR gates.

12. Compare TTL, CMOS and ECL logic families.

13. Explain the working of CMOS NAND gate with a circuit diagram.

14. Draw the 2's comlement parallel adder subtractor and explain its operation.

15. Draw and explain the operation of 4×1 multiplexer.

16. Draw and explain the level clocked Dand T flipflops with truth tables.

17. Draw and explain 4-bit synchronous counter.

18. Explain the working of ring counter and list its applications.

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