



C14-EE-505

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BOARD DIPLOMA EXAMINATION, (C-14)
OCT/NOV—2016
DEEE—FIFTH SEMESTER EXAMINATION
DIGITAL ELECTRONICS

Time : 3 hours]

[Total Marks : 80

PART—A

3×10=30

- Instructions :** (1) Answer **all** questions.
(2) Each question carries **three** marks.
(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. Distinguish between weighted and unweighted codes.
2. Draw the symbols of the following two-input logic gates :
 - (a) AND
 - (b) OR
 - (c) NAND
3. Compare between the TTL, CMOS and ECL logic families.
4. List any three IC numbers of two-input digital IC logic gates.
5. Define the following characteristics of digital ICs :
 - (a) Fan-out
 - (b) Noise margin
6. Draw the full-adder using two half-adders and OR gate.

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7. Compare the performance of serial adder with parallel adder.
8. State the need of preset and clear inputs of flip-flops.
9. Draw the NAND latch and write its truth table.
10. Distinguish between RAM and ROM.

PART—B

10×5=50

Instructions : (1) Answer *any five* questions.
 (2) Each question carries **ten** marks.
 (3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. (a) Briefly explain the significance of parity bit. 3
 (b) Subtract the 45_{10} from 52_{10} using 2's complement method. 4
 (c) Simplify the logic expression $Y = A\bar{B} + \bar{A}B$. 3
12. Draw and explain CMOS NAND gate. 10
13. Draw and explain TTL NAND gate with open collector. 10
14. Draw and explain the decimal to BCD encoder. 10
15. (a) List any three applications of decoders. 3
 (b) Draw and explain the operation of 4×1 multiplexer. 7
- * 16. (a) Distinguish between synchronous and asynchronous counters. 3
 (b) Draw and explain clocked S-R flip-flop using NAND gates. 7
17. Draw and explain 4-bit asynchronous counter. 10
18. (a) Draw and explain the basic principle of working of diode ROM. 6
 (b) Distinguish between EEPROM and UVROM. 4
