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C14–EE–505

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BOARD DIPLOMA EXAMINATION, (C–14)

OCT/NOV—2017

DEEE—FIFTH SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. State de Morgan's theorems.

2. Subtract 101·11 from 1100·1 by using 2's complement method.

3. Define noise margin.

4. Draw the circuit of TTL NAND gate with open collector.

5. Classify digital logic families.

6. List any three applications decoders.

7. Draw the full-adder, using two half-adders and an OR gate.

8. What is the necessity of clock in a flip-flop?

9. Draw the symbol of edge-triggered *D* flip-flop.

10. Compare static RAM and dynamic RAM.

PART—B

10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. *(a)* Draw the symbols of basic gates. 3

(b) Using the *K*-map method simplify the following Boolean function and realize using basic gates : 7

$$Y \quad \overline{A}\overline{B}\overline{C} \quad \overline{A}\overline{B}\,C \quad A\,\overline{B}\overline{C} \quad ABC$$

12. Draw CMOS NAND gate circuit and explain its operation. 10

13. *(a)* Compare TTL, CMOS and ECL logic families. 6

(b) List any four IC numbers of two input digital IC logic gates. 4

14. Draw the 2's complement adder-subtractor and explain its operation. 10

15. Draw decimal to BCD encoder and explain its operation. 10

16. *(a)* Draw *T* flip-flop using *J-K* flip-flop and write its truth table. 6

(b) Explain the importance of **preset** and **clear** inputs. 4

17. Draw and explain 4-bit asynchronous counter. 10

18. *(a)* Draw and explain the working of 4-bit shift right register. 6

(b) Explain the working principle of NV RAM. 4

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