6234

BOARD DIPLOMA EXAMINATION, (C-16)

MAY/JUNE—2023

DECE - THIRD SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time: 3 Hours] [Total Marks: 80

PART—A

 $3 \times 10 = 30$

Instructions: (1) Answer **all** questions.

- (2) Each question carries **three** marks.
- (3) Answers should be brief and straight to the point and shall not exceed five simple sentences.
- 1. Convert the following decimal numbers into binary numbers :
 - (a) $(84.6)_{10} = ()_{2}$
 - (b) $(26.14)_{10} = ()_2$
- 2. Subtract 101010 from 110111 using 2's complement method.
- 3. State De Morgan's theorems.
- **4.** Classify different logic families.
- **5.** Draw full adder circuit using two half adders and an OR gate.
- **6.** Write any three differences between serial adder and parallel adder.
- **7.** List any three applications of flip-flops.
- **8.** Write any three differences between synchronous and asynchronous counters.
- **9.** Draw the symbols of T and D flip-flops and write their truth tables.
- 10. Write any three differences between EEPROM and UVEPROM.

/6234 1 [Contd...

Instructions: (

- (1) Answer *any* **five** questions.
- (2) Each question carries ten marks.
- (3) Answers should be comprehensive and criterion for valuation is the content but not the length of the answer.
- **11.** Realize AND, OR, NOT operations using (a) only NAND gates and (b) only NOR gates.
- **12.** Minimize the following expression using Karnaugh map technique and realize the result with logic gates :

$$Y = A\bar{B}C + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}BC$$

- **13.** Explain the working of open collector TTL NAND gate with a circuit diagram.
- **14.** Draw 4-bit parallel 2's complement adder/subtractor circuit and explain its working.
- **15.** Explain the working of 3×8 decoder with circuit diagram.
- **16.** Draw and explain the working of 4-bit decade counter with a diagram. 10
- **17.** (a) Explain level clocked JK flip-flop with truth table. 7
 - (b) What is race around condition? How to avoid it?
- 18. Draw and explain the working of 4-bit shift left register with a diagram. 10

 $\star\star\star$

/6234 AA23–PDF