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C16–EC–403

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BOARD DIPLOMA EXAMINATION, (C–16)

MARCH/APRIL—2018

DECE—FOURTH SEMESTER EXAMINATION

MICROPROCESSORS

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.
(2) Each question carries **three** marks.
(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. List any six features of 8085 microprocessor.

2. Define Fetch cycle and Execution cycle.

3. State the need of memory segmentation.

4. Calculate the 20-bit physical address for code segment having base address 1234H and offset address 4567H.

5. Classify the instruction set of 8086.

6. List any three data transfer instructions of 8086.

7. Write an 8086 assembly language program to perform 2's complement of an 8-bit number stored in1234H. Store the result in the location 1235H.

8. State the function of RETURN instruction.

9. List any six features of Pentium microprocessor.

10. List the operating modes of 80386.

PART—B

10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. Draw the functional block diagram of 8085 and state the function of each block.

12. *(a)* Draw the pin diagram of 8086. 5

(b) Explain the concepts of sequential processing and pipelining. 5

13. *(a)* Draw the timing diagram of memory read cycle of 8086 in minimum mode. 5

(b) Explain the interrupt response in 8086 microprocessor. 5

14. List the addressing modes of 8086 and explain them with example.

15. Explain the following instructions of 8086 :

(a) XCHG

(b) AND AX, BX

(c) ROL

(d) JC label

16. *(a)* Describe any five assembler directives. 5

(b) List any two assembly language development tools and describe them. 5

17. Draw and explain the architecture of 80486 microprocessor.

18. *(a)* Compare RISC and CISC. 5

(b) Describe instruction level parallelism. 5

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