



C16-EE-305

6241

**BOARD DIPLOMA EXAMINATION, (C-16)
MARCH/APRIL—2025
DEEE – THIRD SEMESTER EXAMINATION**

ELECTRONICS ENGINEERING—I

Time : 3 Hours]

[Total Marks : 80

PART—A

3×10=30

Instructions : (1) Answer **all** questions.
(2) Each question carries **three** marks.
(3) Answers should be brief and straight to the point and shall not exceed five simple sentences.

1. Draw the characteristics of Zener diode.
2. Plot the input and output characteristics of a transistor in CB configuration.
3. Draw the block diagram of DC voltage regulated power supply.
4. List the types of filters.
5. List the applications of solar cell.
6. Plot the drain characteristics of *n*-channel JFET.
7. Draw the circuit of potential divider type of biasing a transistor.
8. Define bandwidth.
9. Define feedback factor.
10. Write any three applications of emitter follower.

PART—B

10×5=50

Instructions : (1) Answer *any* **five** questions.
(2) Each question carries **ten** marks.
(3) Answers should be comprehensive and criterion for valuation is the content but not the length of the answer.

11. Explain the working of PN junction diode with no bias, forward bias and reverse bias conditions.
12. Draw and explain the working of full wave bridge rectifier with wave forms.
13. Draw and explain the working of UJT with V-I characteristics.
14. Explain the construction and working of LCD.
15. Explain collector to base resistor method of biasing a transistor.
16. (a) List the causes of instability of biasing a transistor.
(b) Classify amplifiers based on (i) frequency, (ii) function and (iii) number of stages.
17. Explain the working of two stage transformer coupled amplifier with frequency response curve.
18. Draw and explain the working principle of a single tuned amplifier.

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