C20-CM-302

7235

BOARD DIPLOMA EXAMINATION, (C-20)

NOVEMBER/DECEMBER—2022

DCME – THIRD SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed five simple sentences.

1. Convert $AC6_{(16)}$ into octal.

2. Give the table showing hexadecimal to binary conversion.

3. Construct half-adder using gates.

4. Define NAND gate.

5. Define triggering in the flip-flop.

6. Draw the block diagram of T flip-flop along with its truth table.

7. How asynchronous counter differs from synchronous counter?

8. Define programmable counter.

9. State the purpose of PLA.

10. List any three applications of multiplexers.

PART—B

8×5=40

Instructions : (1) Answer **all** questions.

(2) Each question carries **eight** marks.

(3) Answers should be comprehensive and criterion for valuation is the content but not the length of the answer.

11. *(a)* What are the values of *(i)* $AEF7_{(16)}$ in octal and *(ii)* $8F9A_{(16)}$ in binary?

(OR)

(b) Explain how excess-3 code is constructed from 421 code. Justify your answer in identifying self-complementing code among these two.

12. *(a)* Give the necessary postulates in Boolean algebra and using them prove the De Morgan's theorems.

(OR)

(b) Give the steps of how the 4-variable K-map reduces the given expression $Y = \Sigma m(2,4,5,7,8,10,12,15)$.

13. *(a)* State the reasons for calling NAND and NOR gates as universal gates, explain the working of them with truth tables and diagrams.

(OR)

(b) Construct an adder that adds three bits at a time using half adders only with proper truth tables.

14. *(a)* Give the steps to construct decade counter with truth table.

(OR)

(b) Give the steps to construct universal shift register with diagram.

15. *(a)* Give the steps to construct multiplexer with diagram and truth table.

(OR)

(b) Construct programmable logic array and explain its working principle.

PART—C

10×1=10

Instructions : (1) Answer the following question.

(2) The question carries **ten** marks.

(3) Answer should be comprehensive and the criterion for valuation is the content but not the length of the answer.

16. Reconstruct a parallel adder as 2's complement subtractor with circuit diagrams.

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