7241

BOARD DIPLOMA EXAMINATION, (C-20)

MAY—2023

DECE - THIRD SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours]   [*Total Marks* : 80

PART—A   3×10=30

Instructions : (1) Answer **all** questions.

           (2) Each question carries **three** marks.

           (3) Answers should be brief and straight to the point and shall not exceed five simple sentences.

1. Compare weighted codes with unweighted codes.

2. Construct OR gate using NAND gates.

3. State the importance of parity bit.

4. Define the terms propagation delay and noise margin.

5. Show that two half-adders and OR gate constitute a full-adder.

6. Mention any three applications of decoders.

7. State the need for tri-state buffer.

8. Draw the symbols and truth tables of D and T flip-flops.

9. List any three applications of shift registers.

10. Classify different types of semiconductor memories.

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Instructions : (1) Answer **all** questions.

(2) Each question carries **eight** marks.

(3) Answers should be comprehensive and criterion for valuation is the content but not the length of the answer.

11. *(a)* Explain the working of open collector TTL NAND gate with circuit diagram.

(OR)

(b) Compare the TTL, CMOS and ECL logic families.

12. *(a)* Explain the working of 4-bit parallel adder using full-adders with circuit diagram.

(OR)

(b) Draw and explain the working of 4 × 1 multiplexer with circuit diagram.

13. *(a)* Explain with circuit diagram the operation of asynchronous decade counter.

(OR)

(b) Explain the working of 4-bit shift right register with circuit diagram.

14. *(a)* Draw and explain the working of 3-bit up-down counter.

(OR)

(b) Explain the edge triggered D flip-flop with the help of truth table and circuit diagram.

15. *(a)* Explain the working of basic dynamic MOS RAM cell with circuit diagram.

(OR)

(b) *(i)* Compare EEPROM with UVPROM.

(ii) State any three uses of SD card.

Instructions : (1) Answer the following question.

(2) The question carries **ten** marks.

(3) Answer should be comprehensive and the criterion for valuation is the content but not the length of the answer.

16. When designing a circuit to emulate a truth table such as this, where nearly all the input conditions result in "1" output states. It is easier to use product of sums (POS) expressions rather than sum of products (SOP) expressions.

A	B	C	Output
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Is it possible to use a K-map to generate the appropriate POS expression for the above truth table or K-maps limited to SOP expressions only? Justify your answer.

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