Code No: 113BS

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, March - 2017
DIGITAL LOGIC DESIGN
(Computer Science and Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Solve for X in the equation $(19.125)_{10}=(X)_8$. [2]
b) Demonstrate by means of truth table the validity of the DeMorgan laws. [3]
c) Implement Ex-OR with NOR gates. [2]
d) Find the min terms of wxy+yz+x′y. [3]
e) Design a 4×1 multiplexer. [2]
f) How a decoder can be used like DeMux? [3]
g) What are direct inputs in a flip-flop and why they are used? [2]
h) What is race around condition? How it is eliminated? [3]
i) What are the different type of ROMs? [2]
j) Draw the PLA block diagram. [3]

PART-B

(50 Marks)

2.a) Find 9's complement of 9254.
b) Convert F(A,B,C,D)= Π(0,1,2,3,4,6,12) to the other canonical form.
c) Encode the information character 01101110101 according to the 15 bit Hamming code. [2+4+4]

OR

3.a) Represent $(524)_{10}$ in 2421 code and BCD Excess-3 code.
b) Simplify x+xyz+yzx′+wx+w′x+x,y using Boolean algebra.
c) Draw the logic diagram of (A+B)(C+D)(A'+B+D) without simplifying [2+4+4]

4.a) Find F′ in POS form for F(A, B, C, D)= Π(1, 3, 7, 11, 15) +d(0, 2, 5).
b) Simplify the function F(A,B,C,D)=∑ (0,1,3,4,6,8,15) using K-Map. [5+5]

OR

5. Simplify the function A′B′CE′+A′B′C′D′+B′D′E′+B′CD′+CDE′+BDE′ using K-Map and implement using two level AND-OR gates. [10]

6. Design a BCD to Seven segment display circuit using decoder. [10]

OR

7.a) Construct a 4-bit Ripple Adder and explain.
b) Design a 2-bit magnitude comparator. [5+5]

8.a) What is a Master-Slave flip-flop? Explain with block diagram and logic diagram.
b) Design a divide by 6 Ripple Counter using JK flip-flops. [5+5]

OR

9.a) What is the difference between edge triggering and level triggering? Explain about Edge triggered D flip-flop with a neat diagram.
b) Design a BCD counter with JK flip-flops. [5+5]

10.a) Given a 32×8 ROM chip with enable input, construct a 128×8 ROM with four chips and decoder.
b) Obtain the PLA program table to realize $F_1(x, y, z) = \sum(2, 4, 6, 7)$ and $F_2(x, y, z) = \sum(0, 3, 4, 5)$. [5+5]

OR

11. Implement the following Boolean functions using PLA: [10]
$F_1(A,B,C) = \Sigma(1,2,4,6)$ $F_2(A,B,C) = \Sigma(0,1,6,7)$
$F_3(A,B,C) = \Sigma(2,6)$ $F_4(A,B,C) = \Sigma(1,2,3,5,7)$.

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