R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, February/March - 2016
SWITCHING THEORY AND LOGIC DESIGN
(Common to ECE, EIE, ETM)

Time: 3 Hours   Max. Marks: 75

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A   **[25 Marks]**

1.a) Determine the possible base of the numbers in the operation 302/20=12.1.   [2]
 b) Reduce the expression A'B(D'+C'D)+B(A+A'CD) to one literal.   [3]
 c) What are static hazards ?   [2]
 d) Construct full adder using decoder.   [3]
 e) What is the difference between characteristic table and excitation table?   [2]
 f) Show the characteristic equation for the true output of JK flip-flop is
    $Q(t+1)=JQ'+K'Q$ [3]
 g) How many bit counter is needed to to provide a clock with cycle time of
    50ns if the clock generator produces pulses at a frequency of 80 MHz?   [2]
 h) Compare Synchronous and Asynchronous counters.   [3]
 i) What are compatible states?   [2]
 j) Explain the difference between ASM and conventional flow chart with respect
    to timing.   [3]

PART- B   **[50 Marks]**

2.a) State De-Morgan laws.
 b) Perform the following arithmetic operations in binary using signed 2's complement
    representation for negative numbers   (i) (+62) + (-23)   (ii) (-62) - (-23).
 c) Encode the information character 01101110101 according to the 15 bit Hamming.
                                                                                       [2+4+4]
OR
3.a) Obtain the 1's and 2's complement of the binary numbers 10000000 and 0000001.
 b) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa.
 c) Obtain the truth-table of the function (xy+z)(y+xz) and express the function in sum of
    min terms and product of max terms.   [2+4+4]

4.a) For the function F(w,x,y,z)=$\sum$(1,2,3,5,13) + $\sum\varphi$(6,7,8,9,11,15), find the minimal sum
    of products and product of sums expression.
 b) Implement the function F(A,B,C,D)=$\sum$ (0,1,3,4,6,8,15)   using 4x1 MUX.   [5+5]
OR
5.a) Design a 3-input majority circuit using Multiplexer whose output is equal to 1 if the
    input variables have more 1's than 0's. The output is 0 otherwise.
 b) Find the min terms of the function wxy+x'z'+w'xz by plotting the function in a map.
                                                                                       [5+5]
6.a) Compare Sequential and Combinational circuits.
 b) Design a JK flip-flop using Dflipflop, 2-to-1 line MUX and inverter.   [4+6]

OR

7.a) What is the difference between a latch and flip-flop?
 b) Explain the positive edge triggered D flip-flop with asynchronous reset.   [4+6]

8.a) A sequential circuit with two D flip-flops A and B, two inputs x and y; and one output z is specified by A(t+1)=x'y+xA, B(t+1)=x'B+xA, z=B. Draw the logic diagram and list the state table. Draw the state diagram.
 b) What is a universal shift register?   [8+2]

OR

9.a) Design a counter using T flip-flops with repeated sequence 0,1,3,7,6,4.
 b) Show that a Johnson counter with n flip-flops produces a sequence of 2n states. [5+5]

10.a) Draw the multilevel NAND circuit for expression $F = (AB' + CD')E + BC(A + B)$
 b) Reduce the given expression to a minimum number of literals:
 i) $\overline{(BC' + A'D)}\ \overline{(AB' + CD')}$
 ii) $AB' + CD\overline{(A + B)}$.   [5+5]

OR

11.a) Find the equivalence partition and corresponding reduced machine in standard form.

PS	NS,Z	
	x=0	x=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

 b) Explain the control implementation using MUX.   [6+4]

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