

Code No: 113BU

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, March - 2017

SWITCHING THEORY AND LOGIC DESIGN

(Common to ECE, EIE)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two parts A and B.
 Part A is compulsory which carries 25 marks. Answer all questions in Part A.
 Part B consists of 5 Units. Answer any one full question from each unit.
 Each question carries 10 marks and may have a, b, c as sub questions.

PART- A**(25 Marks)**

- 1.a) Convert the following decimal numbers into their binary equivalents: $(79.515)_{10}$ and $(66.38)_{10}$ [2]
- b) What is an un-weighted code? Represent the decimal numbers 0 to 15 using Gray codes. [3]
- c) What is the significance of priority encoder? [2]
- d) What is hazard? Using an example show how hazard free circuit is realised? [3]
- e) List out the characteristics of flip-flops. Explain any two. [2]
- f) Tabulate the excitation tables of T and D flip-flops. [3]
- g) Define State reduction and State assignment. [2]
- h) What is Lock-out condition in Counters? How to avoid it? [3]
- i) How do you indicate Moore outputs and Mealy outputs in an ASM block? [2]
- j) Briefly Explain FSM capabilities and limitations. [3]

PART-B**(50 Marks)**

- 2.a) Obtain the Dual of the following Boolean expressions.
 - i) $AB + A(B+C) + B'(B+D)$
 - ii) $A + B + A'B'C$
 - b) Obtain the complement of the following Boolean expressions.
 - i) $A'B + A'BC' + A'BCD + A'BC'D'E$
 - ii) $ABEF + ABE'F' + A'B'EF$
 - iii) $ABC + A'BC + AB'C + ABC'$ [4+6]
- OR**
3. For the given three variable Boolean expressions $f(x, y, z) = \pi M (1,3,5,7)$
 - a) Draw the logic circuit for original expression using Basic Logic gates
 - b) Reduce the Boolean expression using Boolean algebra
 - c) Draw the logic circuit for the reduced expression using basic logic gates
 - d) What is your observation after solving (a) and (c). [10]
 - 4.a) Design a full adder and also implement it using multiplexer.
 - b) Simplify the given expression using Quine - McCluskey method
 $f(w, x, y, z) = \sum m(2, 4, 5, 9, 12, 13)$. [5+5]
- OR**
- 5.a) Using K-map obtain the minimal SOP expression for the given switching function and implement it using AND-OR logic.
 $f(A, B, C, D, E) = \sum m (0, 1, 2, 3, 16, 17, 18, 19)$
 - b) Design a 3 to 8 decoder circuit using 2 to 4 decoder circuits. [5+5]

- 6.a) With a neat diagram explain operation of SR flip-flop and derive its truth table, characteristic equation and excitation table? [6+4]
 b) Convert an SR flip-flop into D flip-flop using standard procedure? [6+4]
- OR**
- 7.a) With a neat diagram explain operation of JK flip-flop and derive its truth table, characteristic equation and excitation table? [6+4]
 b) Realize a T flip-flop using JK flip-flop using standard procedure. [6+4]
8. Design a Mod-8 Synchronous UP/DOWN Counter and implement it using T flip-flop. [10]
- OR**
- 9.a) Design a Mod-6 synchronous up-counter using D flip-flops. [5+5]
 b) Design a 4-bit bidirectional shift register using JK flip-flops having right and left data inputs and Mode control M such that M=0 left shift, M=1 right shift. [5+5]
10. Draw the ASM chart for the following state transition, start from the initial state T₁, then if xy=00 go to T₂, if xy=01 go to T₃, if xy=10 go to T₁, otherwise go to T₃. [10]
- OR**
11. A clock mode sequential circuit has to provide z=1 whenever the input completes the Sequence of pulses 1010 and overlapping is allowed. Draw the state diagram and obtain minimal state using partition method. [10]