Code No: 114AF **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, October/November - 2016

DIGITAL DESIGN USING VERILOG HDL

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART - A **(25 Marks)**

1.a)	Define Keywords and Identifiers.	[2]
b)	Define parameters and memory operators.	[3]
c)	Define strengths and content resolution.	[2]
d)	What is continuous assignment structure?	[3]
e)	Explain assignments with delays.	[2]
f)	Draw a simulation flow chart.	[3]
g)	Explain the operation of PMOS switch.	[2]
h)	Explain basic transistor switches.	[3]
i)	Explain capacitive model.	[2]
j)	What is sequential circuit testing?	[3]

PART – B **(50 Marks)**

2. Explain with examples about:
a) Display tasks b) Strobe tasks c) Monitor tasks. [3+3+4]

OR

3.a) Using example, explain about concurrent and procedural statement with syntaxes.
b) Explain the components of a Verilog module with block diagram. [5+5]

4.a) Write a Verilog code for tri-state devices.
b) Explain clocked RS filp-flop Verilog module and test bench. [5+5]

OR

5.a) Design a Verilog module of a 4-bit bus switcher at the data flow level.
b) Explain about operator priority with examples. [5+5]

6.a) Explain blocking and non-blocking statement with examples.
b) Write Verilog code using case statement for any one example. [5+5]

OR

7.a) Explain event construct in a module.
b) Explain stratified event queue. [5+5]

8.a) Design Verilog module for CMOS filp-flop.
b) Explain about module paths. [5+5]

OR

9.a) Explain overriding parameters.
b) Design Verilog module using path delay. [5+5]

10.a) What are the various sequential memory storage models? Explain in detail.
b) How the memory initialization carried out in Verilog? Explain with the help of an example. [5+5]

OR

11.a) With the help of an example explain about the resetting sequence of controller.
b) Write a test bench for moore detector to control the delay. [5+5]