Code No: 115AH

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech III Year I Semester Examinations, February/March - 2016
IC APPLICATIONS
(Electrical and Electronics Engineering)

Time: 3 hours   Max. Marks: 75

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

Part- A

(25 Marks)

1.a)   Draw the interfacing circuit of CMOS driving TTL gate.   [2]
  b)   Why Integrated circuits are needed?   [3]
  c)   List all ideal characteristics of Op-amp.   [2]
  d)   What is the effect of negative feedback in non-inverting amplifier?   [3]
  e)   What are the advantages of active filters?   [2]
  f)   What is VCO? Discuss.   [3]
  g)   What are the basic building blocks of PLL?   [2]
  h)   What are the basic differences between the two operating modes of the 555 timer?[3]
  i)   What is the advantage of R-2R ladder D/A converter over the one with binary
       weighted resistors?   [2]
  j)   What are the different types of ADCs and compare them in terms of speed of operation.
                                                                               [3]

Part-B

(50 Marks)

2.   Draw the circuit diagram of TTL NAND gate and explain its working with the help of
     functional table.   [10]

OR

3.   Draw the circuit diagram of CMOS transmission gate and explain its working.   [10]

4.a)   The op-amp is configured as an inverting amplifier with $R_1=1k\Omega$ and $R_f = 10k\Omega$.
       Calculate exact closed loop gain, ideal closed loop gain and compare these two results.
  b)   Draw the differential amplifier circuit using op-amp and explain its working.   [5+5]

OR

5.a)   Design a subtractor circuit whose output is equal to the difference between the two
       inputs. Use a basic differential op-amp configuration.
  b)   Draw the circuit diagram of an Instrumentation amplifier and explain its working. [5+5]

6.   Design a second order High pass active filter with cutoff frequency of 2 kHz and also
     draw its frequency response.   [10]

OR

7.   Draw the circuit diagram of quadrature oscillator and derive the equation for frequency
     of oscillations and also design such a circuit to generate oscillations at a frequency of
     159 Hz.   [10]

8.a)   Draw the functional block diagram of 555 timer and explain its operation.
  b)   What are the applications of 555 timer and explain any one application in detail.   [5+5]

OR

9.a) Explain the role of Low pass filter and VCO in PLL.
  b) How PLL is used for frequency multiplier? Explain.   [5+5]

10.a) For the D/A converter using an R-2R ladder network, determine the size of each step if
      $R_f = 27k\Omega$ and $R = 10k\Omega$ and also calculate the output voltage when the inputs b_0, b_1, b_2
      and b_3 are at 5V.
  b) Draw the circuit diagram of binary-weighted resistor DAC and explain its working.
                                                                            [5+5]
                                    OR
11.a) Draw the circuit diagram of Dual slope ADC and explain its working.
  b) What is the role of DAC in successive approximation ADC?   [5+5]

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