

Code No: 124BU

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, March - 2017
SWITCHING THEORY AND LOGIC DESIGN
(Common to ECE, EIE, ETM)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

PART- A**(25 Marks)**

- 1.a) What are the different binary codes? [2]
- b) State and prove the Transposition theorem. [3]
- c) Define Essential prime implicant. [2]
- d) What is the procedure to design the combinational circuits? [3]
- e) Differentiate between flip flop and Latches. [2]
- f) What is race around condition? [3]
- g) Give the advantages and disadvantages of Ring Counter. [2]
- h) What do you mean by State table? [3]
- i) How do you obtain the maximal compatibles from the merger table? [2]
- j) What are features of ASM chart? [3]

PART-B**(50 Marks)**

- 2.a) Perform the XS-3 subtraction for the following using 9's and 10's complement methods $96.235_{10} - 125.68_{10}$.
- b) Implement the Hamming code if the receiver receives the data bits as 10100101. [5+5]

OR

- 3.a) How many logic gates are require implementing the following function.
 $F = AB'C + A'BCD + E'F' + ADF$.
- b) Obtain the SOP of $A + BC' + ABD' + ABCD$. [5+5]
- 4.a) Simplify the Boolean Expression $f = \sum m(0,1,2,5,6,7,9,11,12,13,14,15,17,21,27,29,31)$ in SOP and POS using mapping method.
- b) Obtain the set of prime implicates from the Boolean Expression $f = \sum m(0,1,2,5,6,7,8,9,10,12,13,14,15)$ and realize into NAND logic. [5+5]

OR

- 5.a) Design code converter for 4bit BCD to 4bit XS-3.
- b) The circuit receives 4 bit 5211 BCD code. Design the minimum circuit to detect the decimal numbers 1,2,3,6,7 and 8. Implement in universal logic. [5+5]

- 6.a) Draw and Explain the operation of pulse triggered SR flip flop.
 b) Convert JK type flip flop to T type flip flop. [5+5]

OR

- 7.a) Discuss about timing and triggering considerations of the flip-flop and explain clock skew.
 b) Compare and Contrast combinational and Sequential Circuits. [5+5]
- 8.a) Design a 4 bit synchronous counter using JK flip flops.
 b) Design divided by 6 ripple down counter that counts down from 7 and use flip flops that are toggle on positive to negative transitions, and take outputs off the Q lead. [5+5]

OR

- 9.a) Design an asynchronous circuits that will pulses received on the N lines only after a complete positive pulse has been received on the M line.
 b) Design pulse train generator to generate the sequence 1100010. [5+5]
10. A Clocked sequential circuit is defined by the following table.
 a) Find equivalence classes using partition method.
 b) Give proper assignment
 c) Design the circuit using D type flip flop. [10]

PS	NS		OUT PUT	
	X=0	X=1	X=0	X=1
A	A	E	1	0
B	A	E	0	0
C	B	F	0	0
D	B	F	0	0
E	C	G	0	1
F	C	G	0	1
G	D	H	0	1
H	D	H	0	1

OR

11. Draw the ASM chart for the following state transitions. State from the initial state T1, then if XY=00 go to T2, if XY=01 go to T3 and design its control circuit using
 a) D flip flop and Decoder
 b) Input multiplexer and register.
 c) Show the exit paths in an ASM block for all binary combinations of control variables X,Y and Z start from an initial state. [10]

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