**R15**

**Code No: 125EB**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B. Tech III Year I Semester Examinations, November/December - 2017**
**LINEAR AND DIGITAL IC APPLICATIONS**
**(Common to ECE, ETM)**

**Time: 3 hours** **Max. Marks: 75**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

**PART - A**

**(25 Marks)**

| | | |
|---|---|---|
| 1.a) | Define input offset voltage. | [2] |
| b) | List features of 741 op-amp. | [3] |
| c) | Discuss about all pass filters. | [2] |
| d) | List the application of 565 PLL. | [3] |
| e) | List different ADC and DACs. | [2] |
| f) | List specifications of DAC. | [3] |
| g) | Which of the parameters decide the fan out and how? | [2] |
| h) | Explain noise margin and propagation delay with respect to CMOS logic. | [3] |
| i) | What is race around condition? How is it avoided? | [2] |
| j) | Explain one application of SR latch. | [3] |

**PART - B**

**(50 Marks)**

2. Draw the circuit diagram of a two input non-inverting type summing amplifier and derive the expression for the output voltage. [10]

**OR**

3. Explain the working of instrumentation amplifier with suitable diagram. [10]

4. Draw the block diagram of 565 PLL and explain about each block. Make circuit connections to track the input signal and explain its operation. [10]

**OR**

5. Design a wide band pass filter with $f_L$=500 Hz and $f_H$ = 2KHz, and a pass band again = 5 for both sections of filter. Also determine the value of Q for the filter. [10]

6. Which is the fastest ADC? Explain the operation and discuss its merits and de-merits. [10]

**OR**

7. With a neat diagram explain the working principle of R-2R ladder type DAC. [10]

8. With neat circuit diagram explain the working of a 4-bit odd parity generator. [10]

**OR**

9. Design 16×1 multiplexer using 4×1 multiplexer. [10]

10. Design a modulo 12 ripple counter using 74×74. [10]

**OR**

11. How many address and data lines are required to access all the locations of dynamic RAM cell arrays specified below? [10]

a) 4M × 4 b) 1M × 1 c) 1M × 4 d) 4M × 1

**---ooOoo---**