Code No: 126VN **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech III Year II Semester Examinations, December - 2018
VLSI DESIGN
(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a)	Write about the Pass transistor.	[2]
b)	Distinguish between Enhancement and Depletion mode transistor action in N-MOS.	[3]
c)	Write about contacts and vias in layout design.	[2]
d)	Write about the 1.2 μm double metal single poly CMOS rules.	[3]
e)	Mention the different forms of Time delays in gate level circuits.	[2]
f)	Explain about Switch logic and its usage.	[3]
g)	Distinguish a synchronous and an asynchronous counters.	[2]
h)	Write a note on Content Addressable Memory.	[3]
i)	What is the need for testing of IC?	[2]
j)	What are the different chip-level Test Techniques?	[3]

PART - B

(50 Marks)

2.a) Explain the CMOS fabrication process in p-well using suitable diagrams.
b) Discuss the effect of threshold voltage on MOSFET current Equations. [5+5]

OR

3.a) Discuss the MOS transistor Characteristics in Depletion and enhancement modes.
b) Write about Alternative forms of pull-up and describe about the NMOS pull-ups. [5+5]

4. Write about the stick diagrams and design a stick diagram for two input N-MOS NAND and NOR gates. [10]

OR

5.a) Distinguish between the Lambda-base rules and Double metal MOS process rules.
b) Draw the neat layout diagrams for NMOS shift register cell. [5+5]

6.a) Explain the formal estimation of CMOS inverter delay rise-time estimation and Fall-time estimation.
b) Write a note on the Wiring capacitance in detail. [5+5]

OR

7.a) Write about the different Alternate gate circuits in detail.
b) Discuss about the Choice of layers for the gate level design. [5+5]

8.a) Explain the working principle of Ripple carry adder using Transmission Gates.
b) Explain about the configurations and applications of SRAM and DRAM cells. [5+5]

OR

9.a) Explain the Principle and structure of Serial-Parallel multiplier.
b) Describe the design procedure for design of a asynchronous counter. [5+5]

10.a) Design a PAL to realize a full Adder circuit.
b) Explain the detailed Architecture of CPLD and its Implementations. [5+5]

OR

11. Write a short note on the following:
a) CMOS Testing
b) Strategies for testing. [5+5]

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