Code No: 134CF **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, December - 2018
SWITCHING THEORY AND LOGIC DESIGN
(Common to EEE, ECE, MCT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Convert the following numbers with the given radix to decimal.
(i) $A1_{16}$ (ii) 61_7 [2]
b) Represent the following decimal number in BCD: 13597; 99880; 93286. [3]
c) Find the complements of the following: (i) x′yz′ +x′y′z (ii) x(y′z′+yz). [2]
d) Implement the function with only NAND gates: F(x,y,z) = Σ(0,6). [3]
e) Differentiate combinational and sequential circuits? [2]
f) Define clock skew. [3]
g) What is state diagram? [2]
h) Differentiate asynchronous and synchronous counters? [3]
i) Differentiate completely specified and incompletely specified sequential machines. [2]
j) Write capabilities and limitations of Finite-State machine. [3]

PART-B

(50 Marks)

2.a) Solve for X
i) $(F3A7C2)_{16} = (X)_{10}$
ii) $(2AC5)_{16} = (10949)_X$
iii) $(0.93)_{10} = (X)_8$
iv) $(4057.06)_8 = (X)_{10}$
b) Subtract 27810 from 49510 using the excess-3 subtractor. [5+5]

OR

3.a) Prove that AB′C+B+BD′+ABD′+A′C=B+C.
b) Expand minterms and maxterm AB′+ABD′+A+ABC′D. [5+5]

4. Simplify using Boolean postulates and verify using K-map the following
a) (x + y′ + xy′) (xy + x′z + yz)
b) (A+B) (A′+C) (B+C) [5+5]

OR

5.a) Realize the expression F=Σm(0,1,3,5,8,11,12,14,15)using 8×1 MUX.
b) Design the full adder circuit using two half adder circuits. [5+5]

6.a) With the block diagram, Truth table, describe the principle operation of edge triggered negative SR flip flop.

b) Explain the operation of 4-stage twisted ring counter with circuit diagram and timing diagram. [5+5]

OR

7.a) With the aid of external logic, convert D type flip-flop to a JK flip-flop.

b) Design a synchronous modulo-12 counter using JK flip flops. [5+5]

8.a) Design a mod-10 Ripple counter using T flip flops and explain its operation.

b) Draw a state diagram of a sequence detector which can detect 101. [5+5]

OR

9. Design a 4 bit ring counter with initial count 1100 loaded in it. Prepare a state table and draw the state diagram including those of unused states and also the output waveforms. [10]

10. For the machine shown, find the equivalent partition and a corresponding reduced machine in standard form. [10]

PS	NS,Z	
	X = 0	X = 1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

OR

11. Design a sequential logic circuit of a 4 bit counter to start counting from 0000 to 1000 and this process should go on. Draw the ASM chart and design the Data processing unit and the control unit. [10]

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