Code No: 138EW **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year II Semester Examinations, September - 2020
SYSTEM DESIGN USING FPGAS
(Electronics and Communication Engineering)

Time: 2 Hours **Max. Marks: 75**

Answer any Five Questions
All Questions Carry Equal Marks
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1.a) Write Verilog module for a positive edge triggered flip-flop with test bench.
b) Explain JK Flip-flop implementation from VHDL code. [7+8]

2.a) Draw Full Adder write a program gate level modeling.
b) Write Verilog module for 4-bit comparator with test bench. [8+7]

3.a) Design Verilog module event construct for a serial data receiver and test bench for the same.
b) Explain schematic diagram of shift register and draw the simulation waveform. [8+7]

4.a) Write the Verilog code for basic functional unit of a dynamic shift register.
b) Explain synthesized schematic diagram of parallel to serial converter. [7+8]

5.a) Write the VHDL code to generate the divided-by-2 clocks.
b) How can, correct the short path problem, explain with necessary diagram. [7+8]

6.a) What are the advantages of having reset and clock circuitry in its own block separated from the rest of the circuits?
b) Explain, how gated clock signal to avoid generating a glitches in design. [8+7]

7.a) Mention the steps to be followed, when designing with FPGAs, a digital system.
b) Why post layout verification is needed? [10+5]

8.a) What are the design trade-offs involving using additional flip-flops versus the serial of buffers?
b) How Net List will be generated? Explain. [8+7]

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