Jntuk 3-1 onlibe bits of Digital System Design & Digital IC Applications for ECE

Q)A VHDL is which type of language--> **Hardware language**
Q)Basic components of VHDL code are--> **Library ,Entity, Architecture**
Q)A Library is a--> **Collection of commonly used piece of code**
Q)A VHDL is simply declaration of a module inputs and outputs--> **Entity**
Q)In design flow after computation next stage is--> **Simulation/verification**
Q)VHDL is an acronym of--> **VHSIC Hardware Description Language**
Q)In VHDL design flow in front-end design steps are--> **Hierarchy-coding-compilation-Simulation/Verification**
Q)In VHDL design flow in back-end design steps are--> **Fitting/place+route-timing/Verification-Synthesis**
Q)In std_logic_1164 : package of the ieee library specifies--> **A Multi-level logic system**
Q)In std_logic_1164 ; std_logic specifies--> **8 levels logic**
Q)In std_logic_1164 ; std_ulogic specifies--> **9 levels logic**
Q)ieee.std logic 1164, 1164 represents standard logic--> **Package**
Q)In VHDL Library syntax--> **LIBRARY library_name;**
Q)From the following which one is coreect--> **use ieee.std_logic_1164.all;**
Q)A VHDL is a place where VHDL compiler stores information about particular design project including intermediate files.--> **Library**
Q)In VHDL library clause the beginning of design files with--> **Library ieee;**
Q)From following select VHDL user defined identifiers--> **Inhibit, X, Y, Bit, Z etc.**
Q)Package std_logic_1164 of library defines--> **Std_logic and Std_ulogic**
Q)Package std_logic_arith of library ieee defines--> **Signed and Unsigned**
Q)In VHDL identifiers are--> **Basic identifiers and extended identifiers**
Q)Ports is used following syntax--> **Entity**
Q)From following select VHDL reserved key words--> **Entity, Port, In, Out etc.**
Q)In VHDL Entity syntax--> **ENTITY entity_name IS**
Q)In VHDL Architecture syntax--> **ARCHITECTURE architecture-name of entity name is**
Q)In VHDL Type declaration--> **Type type-name is (value-list);**
Q)In VHDL Subtype declaration--> **Subtype subtype-name is type-name start to end;**
Q)in VHDL Signal declaration--> **Signal signal-name : signal type;**
Q)Assignment operator in Behavioral--> :=
Q)From following select VHDL predefined integer types operators--> **+, -, /, mod, abs etc.**
Q)From following select VHDL predefined boolean types operators--> **And, or, nand, not ect,**
Q)From following select VHDL data objects--> **Constant, Signal, Variable, File**
Q)From following select VHDL predefined types--> **Bit, Boolean, bit_vector etc**
Q)From the following find the Miscellaneous operators--> **Abs, ** etc**
Q)If x=1001010 than sll2 is--> **0101000**
Q)If x=1001010 than rol2 is--> **0101010**
Q)Statement referred in dataflow--> **Concurrent**
Q)With select syntax--> **With signal name select signal name<= expression when choices;**
Q)From the following find the relational operators--> **=, /=, <, <= etc.**
Q)With select syntax--> **With expression select signal name<= signal value when choices;**
Q)Assignment operator in Behavioral--> **<<**
Q)Concurrent statement is as follows--> **Signal signal-name<= expression;**

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Q)Key word others used in syntax--> **With select**
Q)While loop syntax in behavioral modal--> **While Boolean expression loop Sequential statement End loop;**
Q)Syntax of function--> **Function function-name (concurrent statements)**
Q)Port MAP syntax is--> **Label: Component name port map (signal1, signal2 signal3,.,signal n)**
Q)Is present in between process begin and end process--> **Sequential statements**
Q)Applying inputs to A,B not applied to Y in the program write process--> **Process (A,B)**
Q)Port map is used in following model--> **Structural**
Q)In VHDL Simulation is used for--> **Validate assumptions, Verify logic and Verify performance**
Q)Intermediate files that are not used in VHDL are--> **Operating systems**
Q)A VHDL is allows you to define and apply inputs to your desired and to observe it outputs--> **Simulation**
Q)Logic synthesis is a--> **Logic Synthesis - synthesis of gate-level logic from register-transfer structure or Boolean equations**
Q)To ensure that the design is correct as per the specifications the designer has to write another program known as--> **Simulation**
Q)In VHDL modeling types of simulations are--> **Logic or switch level, Timing, Circuit and Fault**
Q)Generic constants are declared in--> **Entity**
Q)A function executes in minimum simulation time.--> **Zero**
Q)A may or may not execute in zero simulation time depending on whether it has wait statement or not--> **Procedure**
Q)To delay a event by 20 ns in VHDL Program which of the following statement should be given--> **Wait for 20 ns;**
Q)A function executes in minimum simulation time.--> **Zero**
Q)The mechanism makes it possible to simulate the operation of concurrent process even through the simulator runs on single computer with single thread of execution--> **Event list**
Q)A VHDL is allows you to define and apply inputs to your desired and to observe it outputs--> **Simulation**
Q)Following statement in correct time dimension--> **Wait or sensitivity:**
Q)Design a synthesis tools used for--> **Optimize the gate level description using cell substitution to meet the specified area and timing constraints**
Q)Register-Transfer Synthesis is--> **Synthesis of register-transfer structure from abstract, control-flow, or register-transfer behavior**
Q)The automatic generation of data path and control unit is known as high-level synthesis.--> **Synthesis**
Q)Synthesis may occur at many different levels of abstraction are--> **Behavioral level synthesis, Logic synthesis and Layout synthesis**
Q)Data path is a--> **The hardware which stores and performs operations on data**
Q)In VHDL Behavioral synthesis--> **To optimize the design at architectural level with constraints for clock, latency and throughput**
Q)In VHDL Logic synthesis--> **Automatically converts RTL code into gates without modifying the implied**

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Q)In VHDL Verification at different levels of abstraction are--> **Behavioral, RTL, gate level and Physical domain**
Q)In VHDL Behavioral verification is--> **Describes the intent and the algorithm behind the design without specifying the cycle to cycle behavior**
Q)A gate delay is--> **Time for change at input to cause change at output**
Q)The process of mapping an input specification for a hardware design into a hardware implementation--> **Hardware Synthesis**
Q)Different types of Logic Synthesis Constraints are--> **Synthesis Constraints, timing, area, power and Design Rule Constraints**
Q)From following Logic Synthesis Constraints are--> **Timing, area optimization and Limitations of a given implementation technology**
Q)In VHDL model inertial delay is--> **Default delay model**
Q)In VHDL model Delta delay is--> **Infinitesimally small delay is automatically inserted by the simulator to preserve correct ordering of events**
Q)Critical path is a--> **The hardware which stores and performs operations on data**
Q)Type of Delay Models in VHDL are--> **Inertial, Transport and delta delays**
Q)Static Timing analysis after Synthesis is called--> **Pre-Layout Analysis**
Q)Static Timing analysis after place and route is called--> **Post-Layout Analysis**
Q)Post-Layout Timing simulation Flows are--> **Floor planning-Clock Tree Synthesis-Place and Route-Parasitic Extraction-Static Timing Analysis**
Q)In synthesis Optimization Constraints is--> **Define timing and area optimization goals for Design Compiler**
Q)In Logic Synthesis power constraints are--> **Logic synthesis can generate gating that minimizes the number of transitions during operation**
Q)In Logic Synthesis Design Rule Constraints--> **Maximum loading on outputs and Maximum transition time on outputs**
Q)Pre layout simulation Flows are--> **Logic Synthesis- Design For test- Floor planning- Static Timing Analysis**
Q)The advantage of static Timing Simulation is--> **Fast, exhaustive**
Q)In timing simulation a point-to-point path in a design which can propagate data from one flip-flop to another is called--> **A Timing Path**
Q)The advantage of Dynamic Timing Simulation is--> **Can be very accurate**
Q)In VHDL Modeling Verification Techniques are--> **Simulation, Formal verification and Static Timing Analysis**
Q)A method for determining if a circuit meets timing constraints without having to simulate clock cycle is called--> **Static Timing Analysis**
Q)The performance of Static Timing Analysis--> **Timing-driven and Gate-level simulation**
Q)Types of Static Timing Verification are--> **Dynamic and Static Timing Analysis**
Q)Algorithm Synthesis is--> **Synthesis of abstract behavior or control-flow behavior from a high level algorithm description**
Q)A Read only memory is--> **Combinational circuit**
Q)A setup time violation is--> **When a signal arrives too late, and misses the time when it should advance**
Q)In a timing path Input ports Clock pins of flip-flops are called--> **Start point**

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Q)In a timing path output ports data input pins of flip-flops--> **Endpoints**
Q)In Static Timing Analysis which kinds of timing errors are possible--> **Clock period, hold time and setup time violations**
Q)A hold time violation is--> **When a signal arrives too early, and advances one clock cycle before it should.**
Q)From following find the volatile memory--> **RAM**
Q)Which is the type of memory for information that does not change when power off--> **ROM**
Q)For manufacturing of ROM ICs. Which types of Technologies are used--> **Bipolar Technology and MOS Technology**
Q)From the expression of 2^n b ROM, b is represent--> **Data outputs**
Q)From the expression of 328 ROM, Input addresses are--> **5**
Q)ROM is a--> **Nonvolatile memory**
Q)From the expression of 2^n b ROM, 2^n is represents--> **Output address**
Q)In a PAL, the AND and OR arrays are--> **Programmable AND array and fixed OR array**
Q)In a PLA, the AND and OR arrays are--> **AND and OR arrays are programmable**
Q)What does a dot mean when placed on a PLD circuit diagram?--> **A point that cannot change**
Q)Which memory is used for storing programs and data currently being processed by the CPU?--> **Internal memory**
Q)One Gigabyte equal to--> **A Billion**
Q)In a PROM, the AND and OR arrays are--> **Fixed AND array and Programmable OR array**
Q)In a PROM, the OR array is--> **Programmable**
Q)A programmable array of AND gates that connects to a fixed array of OR gates and is usually called--> **PAL**
Q)The basic programmable logic array (PLA) contains a set of _____ gates, _____ gates, and _____ gates.--> **NOT, AND, OR**
Q)Each programmable array logic (PAL) gate product is applied to an OR gate and, if combinational logic is desired, the product is ORed and then:--> **Sent to an inverter for output**
Q)From the following find the wrong one--> **In a PLA , fixed AND array and Programmable OR array**
Q)The difference between a PLA and a PAL is:--> **The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane.**
Q)PALs tend to execute--> **SOP**
Q)Once a PAL has been programmed--> **It cannot be reprogrammed.**
Q)For manufacturing of PROM ICs. Which types of Technologies are used--> **Bipolar**
Q)For manufacturing of EPROM ICs. Which types of Technologies are used--> **CMOS**
Q)For manufacturing of Mask ROM ICs. Which types of Technologies are used--> **NMOS,CMOS**
Q)SPLDs, CPLDs, and FPGAs are all which type of device?--> **PLD**
Q)A PAL16L8 has:--> **10 inputs and 8 outputs.**
Q)The content of a simple programmable logic device (PLD) consists of:--> **Thousands of basic logic gates and advanced sequential logic functions**
Q)Product terms are the outputs of which type of gate within a PLD array?--> **AND**
Q)RAM can be expanded to a--> **Increase word number**
Q)The programs which are as permanent as hardware and stored in ROM is known as--> **Firmware**

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Q)The memory which is programmed at the time it is manufactured--> **PROM**
Q)For manufacturing of EEPROM ICs. Which types of Technologies are used--> **NMOS**
Q)EEPROM stands for--> **Electrically Erasable Programmable Read Only Memory**
Q)EPROM is generally erased by using--> **Ultraviolet rays**
Q)The internal structure of PLA is similar to--> **ROM**
Q)SRAM used for--> **Digital to analog conversion**
Q)SRAM have--> **Does not have to be periodically refreshed**
Q)SRAM provides--> **Faster access to data**
Q)What is the advantages of Two-Dimensional Decoding--> **Reduce the Decoder size**
Q)From the following find the one of the standard SRAM--> **HM628128**
Q)Which of the following memories needs refreshing?--> **DRAM**
Q)In SRAM data is stored in cross-coupled inverters--> **Cross-coupled inverters**
Q)The Access time is slower for--> **SRAM and DRAM**
Q)In Synchronous DRAM ,Memory data path width is--> **4 bytes**
Q)For performing read and write operations, Synchronous DRAM requires--> **Clock**
Q)For the most Static RAM the write pulse width should be at least--> **60ns**
Q)For the most Static RAM the maximum access time is about--> **100ns**
Q)Minimum number of transistor required for designing a DRAM--> **1 Transistor**
Q)Minimum number of transistor required for designing a SRAM--> **G. 6Transistor**