Code No: **R41021** **R10** **Set No. 1**

IV B.Tech I Semester Supplementary Examinations, Feb/Mar - 2015

COMPUTER ORGANIZATION

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1 a) What is the use of compliment operation in digital computers? Explain r's and (r-1)'s complement. [8]

b) Find the actual number from its IEEE 754 representation.
Sign = 0
Exponent = 0011 0100
Mantissa = 0100 0110 0000 0000 0100 000 [7]

2 a) Design Binary Adder/Subtractor circuit and explain its functionality. [8]

b) Explain the hardware implementation of Shift Microopearations. [7]

3 What are the different fields in the instruction format? Evaluate R = (X*Y) + (A-B) arithmetic statement using 0 address, 1 address, 2 address and 3 address instruction formats. [15]

4 a) Explain the micro instruction format and microoperations with example. [8]

b) Explain about micro programmed control organization with neat sketch [7]

5 a) Explain the Memory Hierarchy in computer system with neat sketch. [8]

b) What is the Cache memory? Explain why cache memories improve the system's performance. [7]

6 a) Explain about Input-output interface with an example [8]

b) What is the difference between synchronous and asynchronous data transfer? [7]

7 a) Explain how parallel execution takes place in the pipeline processors. [8]

b) Draw the space time diagram for 5 stage pipeline showing the time required to complete 8 tasks. [7]

8 a) Explain how synchronization is achieved in multiprocessor systems [8]

b) Write a note on multi port memories. Mention its limitations. [7]

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Code No: **R41021** **R10** **Set No. 2**

IV B.Tech I Semester Supplementary Examinations, Feb/Mar - 2015

COMPUTER ORGANIZATION

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

*****

1 a) Find the output binary number after performing the subtraction using 1's complement and 2's complement
i) 10001 - 1100 ii) 111.01 - 010.11 [8]

b) What is a fixed point representation? Explain how to detect overflow in fixed point representation. [7]

2 Design register selection circuit to select one of the four 4-bit registers content on to bus. Briefly explain about register selection circuit with neat sketch [15]

3 a) Explain any four addressing modes in detail with examples. [8]

b) Briefly Explain about RISC. How RISC is advantageous over CISC. [7]

4 a) Design a hardwired control unit for CPU. Why hardwired CU are suitable for RISC. [8]

b) What is meant by mapping of microoperation? Explain. [7]

5 a What is page replacement mechanism? Discuss about LRU algorithms with example. [8]

b Explain about main memory with its hardware organization. [7]

6 a) Explain How Handshaking Asynchronous data transfer is advantageous over strobe control data transfer. [8]

b) Write notes on peripheral devices. [7]

7 a) Describe the characteristics of vector processor systems. [8]

b) Explain about instruction pipelining with neat sketch. [7]

8 a) What is the functioning of cross bar switch network? Explain. With a neat sketch [8]

b) What is cache coherence problem in shared memory multi processor system? Explain. [7]

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Code No: **R41021** **R10** **Set No. 3**

IV B.Tech I Semester Supplementary Examinations, Feb/Mar - 2015

COMPUTER ORGANIZATION

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1	a)	How do we represent the signed integers? Explain with examples.	[8]
	b)	Briefly explain about the structure of the bus in Computer system.	[7]
2		Draw the block diagram of 4-bit arithmentic cicuit and explain the functionality and show in tabular form.	[15]
3	a)	What is an Interrupt? Explain the flowchart Interrupt cycle.	[8]
	b)	Explain different memory reference instructions.	[7]
4	a)	What are the design goals for a designer while deciding a hardwired or microprogrammed CU for a CPU?	[8]
	b)	Explain about address sequencer in Micro programmed CU.	[7]
5		Write a note on Cache memory. Explain three cache–main memory mapping techniques with suitable diagrams.	[15]
6	a)	What is DMA? Explain it with neat diagram.	[8]
	b)	Briefly explain the different modes by which data transfer can take place between a computer unit and its I/O devices.	[7]
7	a)	Specify a pipeline configuration to carry out the task R= (A+B) * (C+D) List the content of all registers in the pipeline for i= 1 through 6.	[8]
	b)	Explain about vector operations.	[7]
8	a)	Briefly explain about interconnection structures in multi processor systems.	[8]
	b)	Explain the characteristics of Multiprocessors.	[7]

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Code No: **R41021** **R10** **Set No. 4**

IV B.Tech I Semester Supplementary Examinations, Feb/Mar - 2015

COMPUTER ORGANIZATION

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1 a) What is meant by normalization in floating point representation? Why do we need it? What normalization is used in IEEE 754 standard? [8]

b) What are functional units? Discuss in detail about basic functional units of a computer? [7]

2 a) Brief the three state bus buffers with neat sketch. [8]

b) Explain about Logic Microoperations. Give its hardware implementation. [7]

3 Explain about basic instruction cycle. Explain are the different phases of instruction cycle with neat diagrams and Draw the flow chart. [15]

4 a) Differentiate Hardwired and Micro programmed control Units [8]

b) What are the horizontal and vertical micro instructions formats, Nano programming. Explain. [7]

5 a) What is page replacement mechanism? Discuss about FIFO algorithms with example. [8]

b) Consider a cache consisting of 256 blocks of 8 words each, for a total of 2048 words, and assume that the main memory is addressable by a 16-bit address. The main memory has 64K words which are divided into 8192 blocks of 8 words each. Find the number of bits in Tag, Block and Word field of the main memory address for direct mapping scheme. [7]

6 a) Explain about asynchronous data transfer using Handshaking protocol. [8]

b) Write a short note on magnetic disks and tapes. [7]

7 a) Explain how branch instructions can be handled in the pipeline processors. [8]

b) Write a note on Array processors. [7]

8 a) Discuss about Flynn's classification of parallel processor systems. [8]

b) Explain about time shared common bus organization. [7]

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